COMPUTER CONTROLLED COMPACT DISC PLAYER

DP-720

SERVICE MANUAL

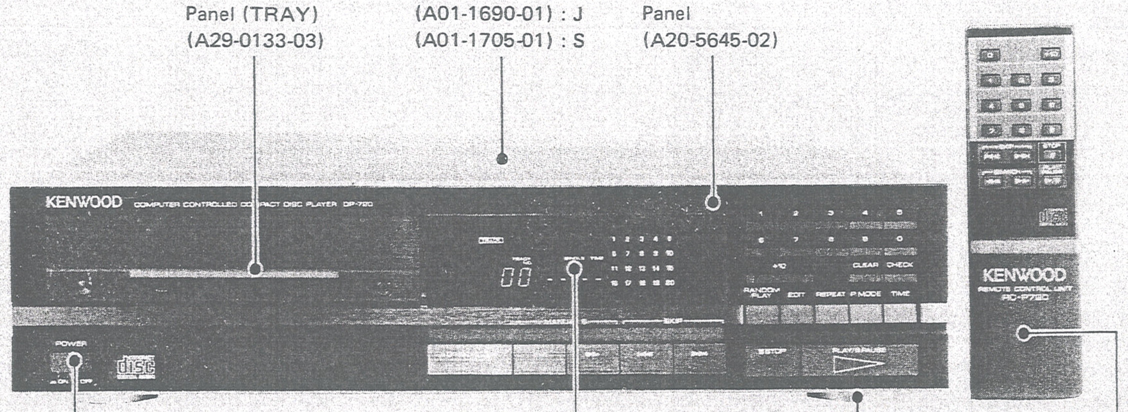
KENWOOD

B51-3600-00(O)1513

Panel (TRAY)
(A29-0133-03)

Metallic cabinet
(A01-1690-01) : J
(A01-1705-01) : S

Panel
(A20-5645-02)



Knob ass'y (POWER)
(K29-3337-03)

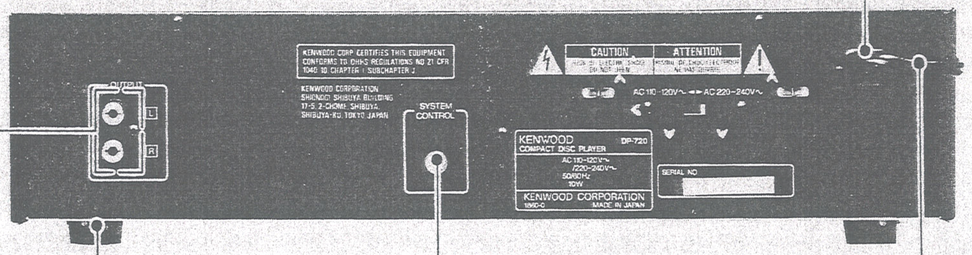
Dressing plate
(B03-2490-04)

Foot (FRONT)
(J02-1003-05)x2

Remote controller ass'y
(A70-0244-05)

Phono jack (2P) OUTPUT
(E13-0235-05)

Power cord bushing
(J42-0166-05) : J
(J42-0083-05) : S



Foot (REAR)
(J02-0170-04)x2

Miniature phone jack (SYSTEM CONTROL)
(E11-0164-05)

AC power cord*
(E30-)

J : Japan made
S : Singapore made

In complicance with Federal Regulations, following are reproductions of labels on, or inside the product relating to laser product safety.

KENWOOD-Corp. certifies this equipment conforms to DHHS Regulations No. 21 CFR 1040. 10, Chapter 1, Subchapter J.

DANGER : Laser radiation when open and interlock defeated.
AVOID DIRECT EXPOSURE TO BEAM.

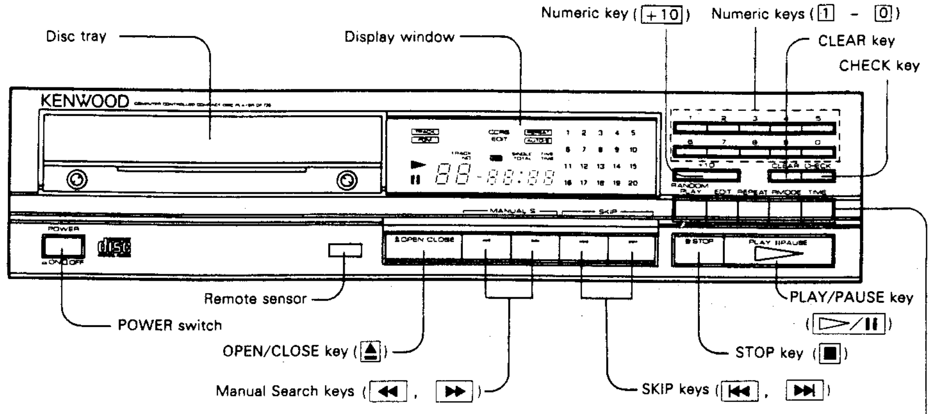
Caution :
The Mechanism ass'y used with the DP-720 varies in two types depending on the manufacturing location. (Japan, Singapore)

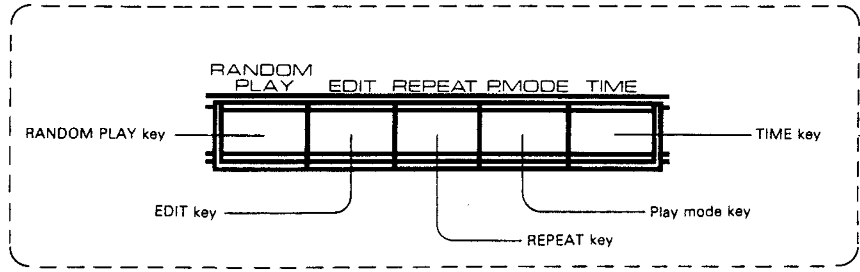
*** Refer to parts list on page 86.**

CONTENTS

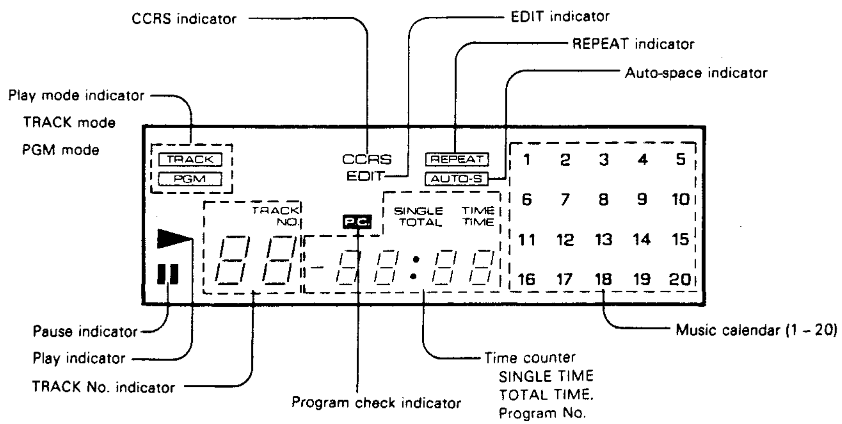
CONTROLS AND INDICATORS

1. Front of Unit





2. Display Window

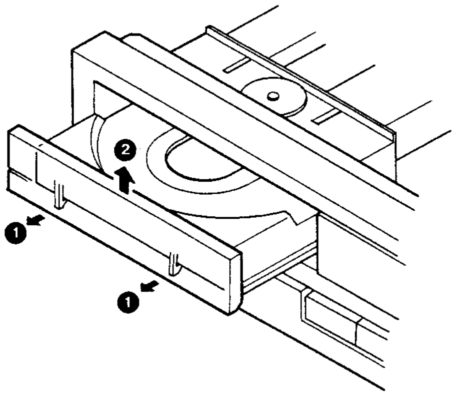


DISASSEMBLY FOR REPAIR (X92-1300-00) JAPAN MADE

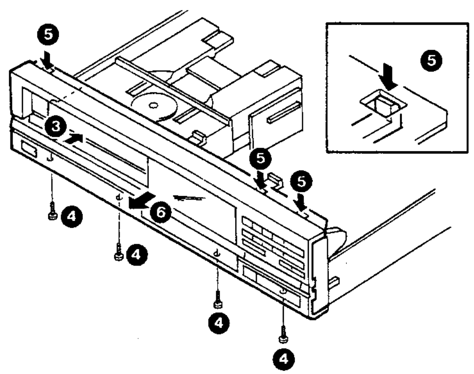
1. Removing the Control Unit

* Remove the case. However, it is not necessary to remove the feet and the holder.

1. Remove the two catches (1), and remove the tray panel by sliding it upward (2).

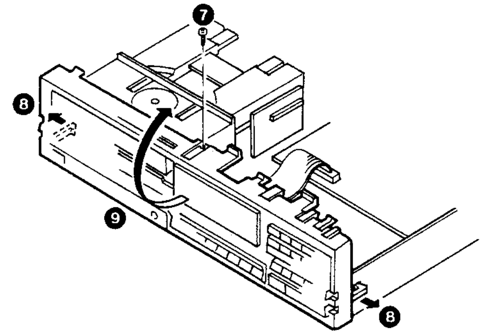


2. Push the tray into the unit (3).
3. Remove the four screws (4) and release the three catches (5) to remove the front panel (6).

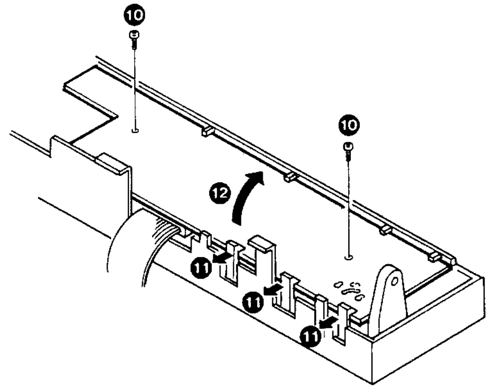


DISASSEMBLY FOR REPAIR (X92-1300-00) JAPAN MADE

4. Remove the screw (7) and release the two catches (8) to remove the sub panel (9).



5. Remove the two screws (10) and release the three catches (11) to remove the control unit (12).



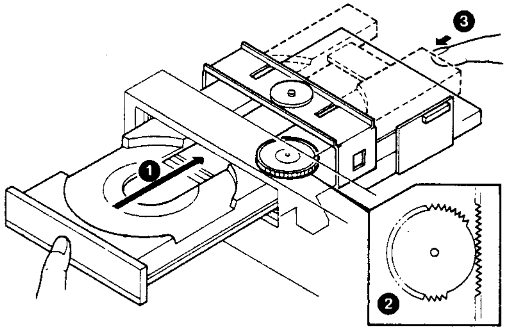
DISASSEMBLY FOR REPAIR (X92-1300-00) JAPAN MADE

2. Removing and Installing the Tray

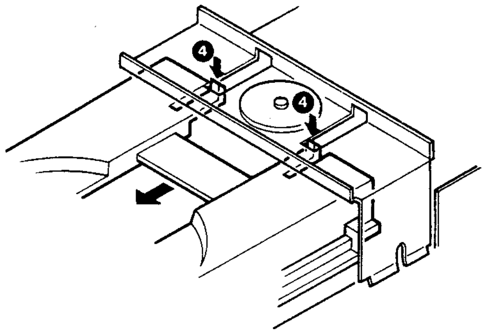
2–1. Removing the Tray

* Open the disc tray and turn the power OFF.

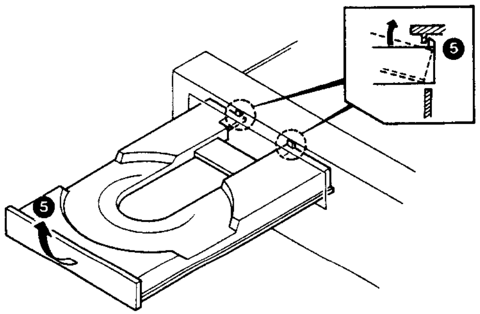
1. Push the tray gradually into the unit (❶) by your hand. In this condition, the gear will be released (❷).
2. Push the rear end of the tray toward the front to remove the tray until it stops (❸).



3. Release the two stoppers (❹) and take out the tray front the unit.



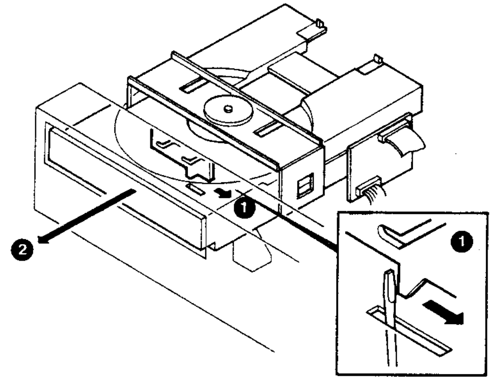
4. When removing the tray, release the stoppers in the direction of the arrow (❺) to prevent it from engaging with the sub panel.



DISASSEMBLY FOR REPAIR (X92-1300-00) JAPAN MADE

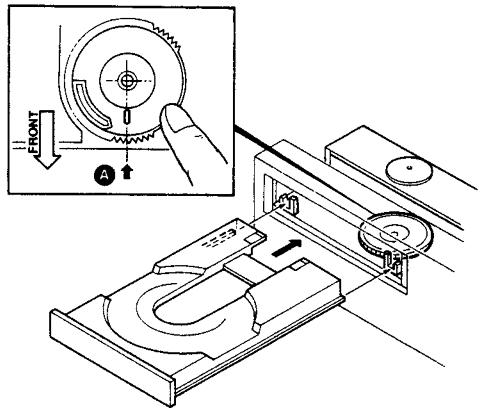
Note : When the power can not be turned ON, or when the tray can not be opened by pressing the OPEN key :

1) Insert the screwdriver into the hole located on the bottom of the unit, as shown in the diagram, and push the lever with the screwdriver (❶).
2) When the tray is comes out slightly, the gear is released. Then take out the tray toward the front (❷).



2–2. Installing the Tray

1. Set the gear to the position (Ⓐ) shown in the diagram.
2. Insert the tray along with the guide rails on the both sides.

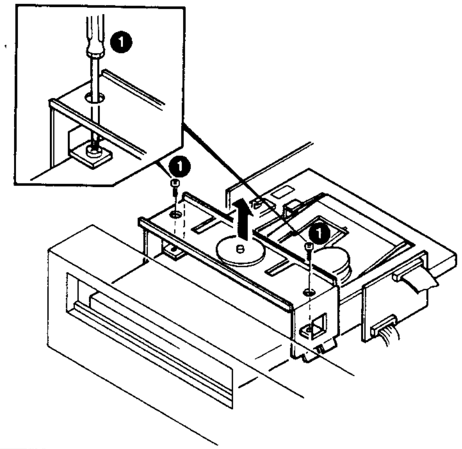


DISASSEMBLY FOR REPAIR (X92-1300-00) JAPAN MADE

3. Removing the Pickup

* Remove the tray .

1. Remove the two screws (1) and remove the catch of the clamper.



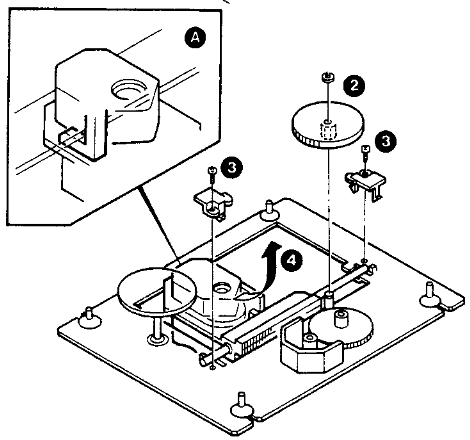
2. Remove the holding fitting and remove the gear (2).
3. Remove the two fixing fittings (3).
4. Remove the pickup in the direction of the arrow (4).

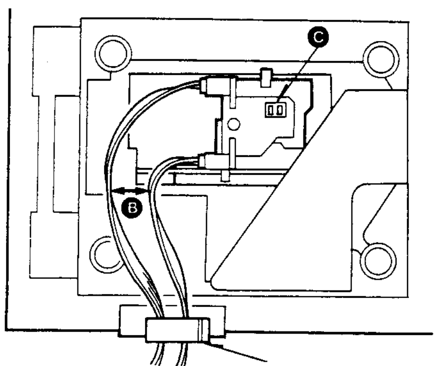
Note 1 : When installing the pickup :

- Install the pickup so that the metal fittings are engaged with the guide of the pickup (A).
- Keep the flat cable from the pickup away from the unit as far as possible (B).

Note 2 : When the pickup has been replaced :

- For the protection of the laser diode (LD), the LD short land of the pickup may be shorted. If so, after connecting the connector, unsolder the short land (C).





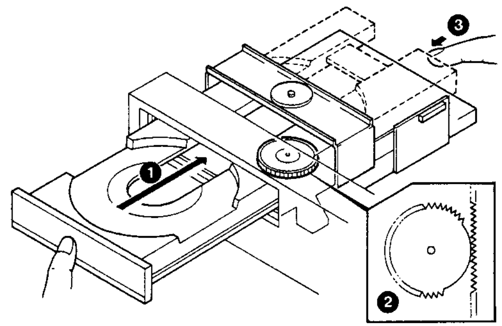
DISASSEMBLY FOR REPAIR (X92-1340-00) SINGAPORE MADE

1. Removing and Installing the Tray

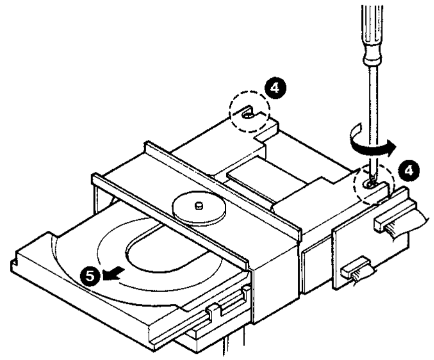
1–1. Removing the Tray

* Open the disc tray and turn the power OFF.

1. Push the tray gradually into the unit (1) by your hand. In this condition, the gear will be released (2).
2. Push the rear end of the tray toward the front to remove the tray until it stops (3).

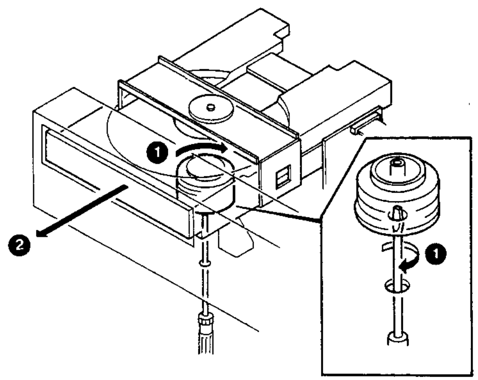


3. Remove the two screws (4) of the tray stopper.
4. Draw out the tray (5).



Note : When the power can not be turned ON, or when the tray can not be opened by pressing the OPEN key :

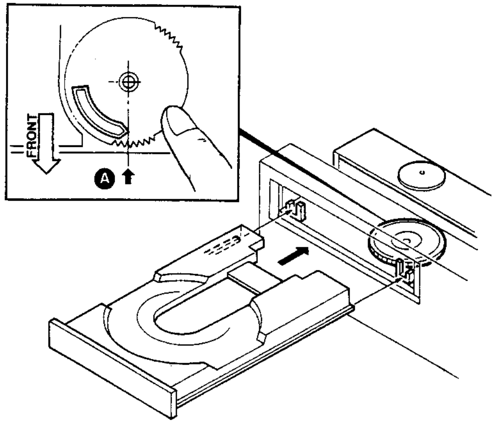
1) Rotate the control cam by a screwdriver, etc. set into the hole on the bottom plate of the unit as shown (1).
2) When the tray is comes out slightly, the gear is released. Then take out the tray toward the front (2).



DISASSEMBLY FOR REPAIR (X92-1340-00) SINGAPORE MADE

1–2. Installing the Tray

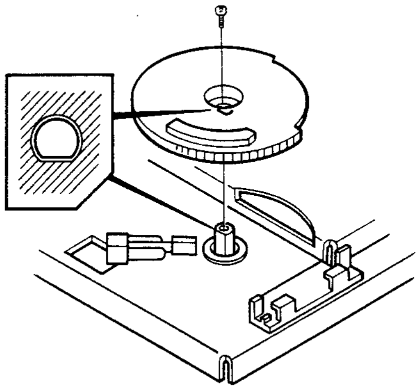
1. Set the gear to the position (A) shown in the diagram.
2. Insert the tray along with the guide rails on the both sides.



2. Installing the Loading Gear

2–1. Installing the Drive Gear

Align the drive gear with the cutout section of the control cam to install it.

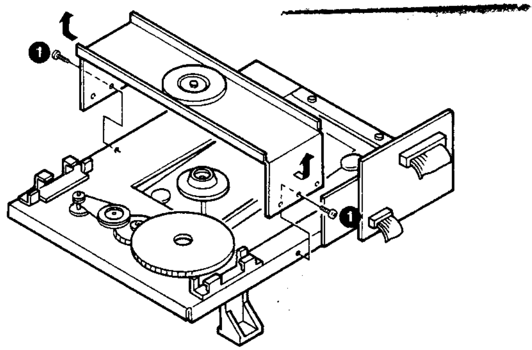


DISASSEMBLY FOR REPAIR (X92-1340-00) SINGAPORE MADE

3. Removing the Pickup

* Remove the tray.

1. Remove the two screws (1) and remove the catch of the clamper.



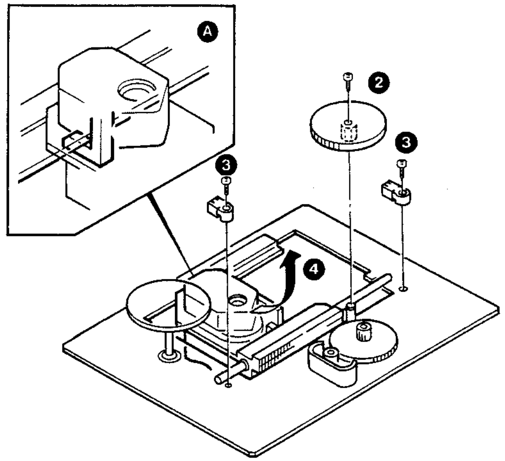
2. Remove one screw and take out the gear (2).
3. Remove the two shaft clamper (3).
4. Remove the pickup in the direction of the arrow (4).

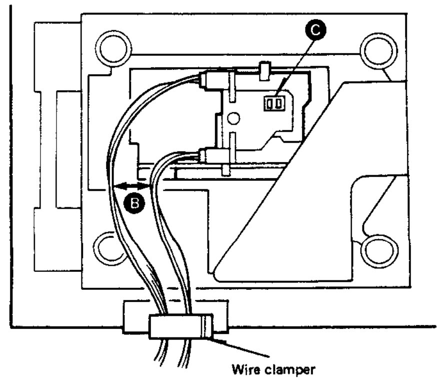
Note 1 : When installing the pickup :

- o Install the pickup so that the metal fittings are engaged with the guide of the pickup (A).
- o Keep the flat cable from the pickup away from the unit as far as possible (B).

Note 2 : When the pickup has been replaced :

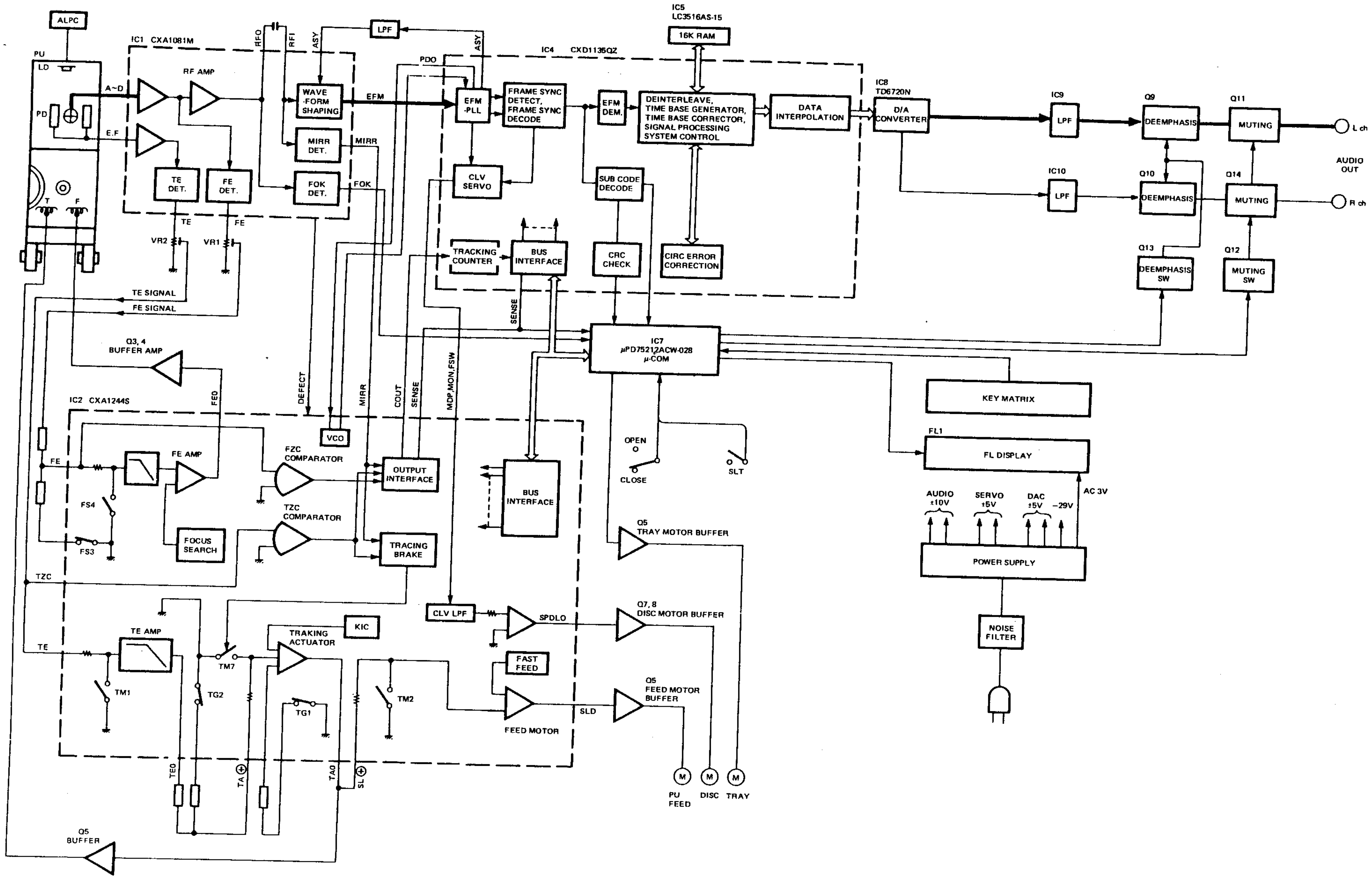
- o For the protection of the laser diode (LD), the LD short land of the pickup may be shorted. If so, after connecting the connector, unsolder the short land (C).





DP-720

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

1. Description of Components

1–1. CONTROL CIRCUIT UNIT (X29-1890-02) : Japan made, (X29-1890-03) : Singapore made

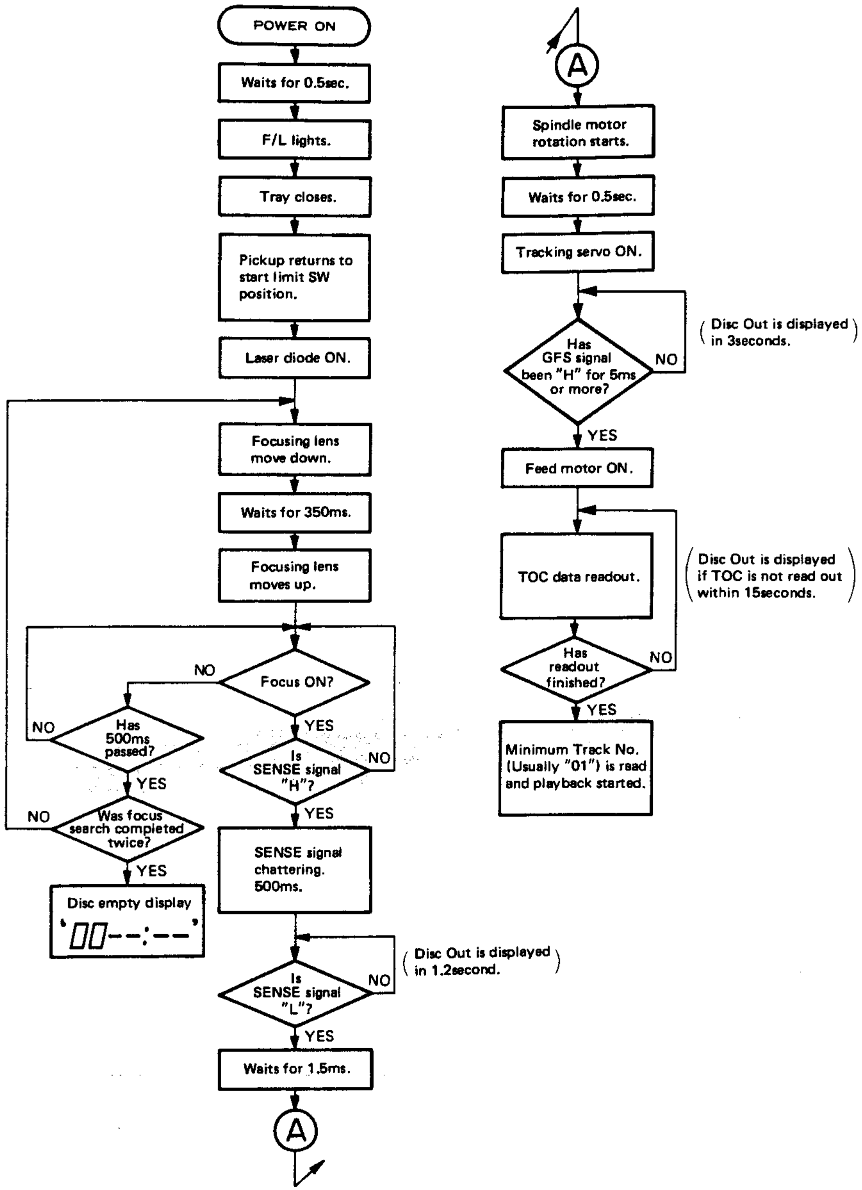
Ref. No.	Parts No.	Use/Function	Operation/Condition/Compatibility
IC1	CXA1081M	RF amp	Focusing error signal generator, tracking error signal generator, RF signal generator and phase comparator, and auto-symmetry corrector circuit.
Q1	2SA1426	Switch	Laser ON/OFF switch.
Q2	2SC945A(Q,P)	Switch	Focusing error amp bias switch.

1–2. CD PLAYER UNIT (X32-1260-23, X32-1262-73) : Japan made, (X32-1302-72) : Singapore made

Ref. No.	Parts No.	Use/Function	Operation/Condition/Compatibility
IC1	TC4066BP	Analog switch	(1) Tracking gain switch. The gain is normal in normal operation, and low when scratch is detected. (2) Tracking servo switch, which receives the scratch detect (DFCT) signal and switches the tracking servo OFF when there is a scratch. (3) Switches the TE signal input from the anti-shock terminal (ATSC, pin 19 of CXA1244S). (4) Digital output ON/OFF switch. On when reset signal is "H".
IC2	CXA1244S	Servo IC	Generation of focusing servo, tracking servo and feed servo pulses for servo control.
IC3	M5218P	Opamp	(1/2) Opamp for tray motor drive. (2/2) Inversion of tracking error phase. (The gain is switches by the opamp and IC1.)
IC4	CXD1135QZ	Digital signal processor LSI	All digital signal processing operations, including the EFM data demodulator, error corrector, interpolation circuit, PLL circuit, CLV servo circuit, digital output circuitry, etc.
IC5	LC3518BSL-15	S-RAM	Signal processing RAM (16K).
IC6	M5218P	Opamp	(1/2) PLL compensation circuit (LPF + amp). (2/2) CLV compensation circuit (LPF + level shifter).
IC7	μPD75212ACW-028	Microprocessor	Display control, key input processing and servo IC control.
IC8	TD6720N	D/A converter	Integrating D/A converter (with built-in sample & hold circuit).
IC9, 10	M5218P	Opamp	7-stage LPF amplifier.
IC11	LM2940CT-5.0	3-terminal regulator	+5V regulated power supply for analog circuitry.
IC12	M5218P	Opamp	(1/2) Used for control of –5V analog circuit power supply. Tracking is performed at the positive-going or negative-going edge of +5V (IC11). (2/2) Generation of RESET signal when power is switched ON/OFF.
Q1	2SA733(A)(Q,P)	Transistor	Inversion of DFCT signal logic.
Q2	2SC945A(Q,P)	Transistor	Amplification of tracking error signal and LPF processing. The output is input to the ATSC (anti-shock) terminal.
Q3	2SD1266	Driver	Focusing coil driver.
Q4	2SA1534A	Driver	Focusing coil driver.
Q5	STA341M	Driver	(1/3) Tray motor driver. (2/3) Feed motor driver. (3/3) Tracking coil driver.
Q6	2SC945A(Q,P)	Transistor	Amplification of 16.9344MHz clock from IC8. The output is input to IC4.
Q7	2SC3940A	Driver	Disc motor driver.
Q8	2SA1534A	Driver	Disc motor driver.
Q9, 10	2SC2878	Switch	Deemphasis ON/OFF switch.
Q11, 12	2SC2878	Switch	Analog audio muting switch.
Q13	2SA733(A)(Q,P)	Switch	Deemphasis level shifter.
Q14	2SC945A(Q,P)	Switch	Analog muting level shifter.
Q15	2SD1944	Ripple filter	Ripple filter for +5V regulated power supply.
Q16	2SA954(L,K)	Ripple filter	Ripple filter for –5V regulated power supply.
Q17	2SA954(L,K)	Ripple filter	Analog circuitry (DAC) power supply voltage control (–5V).
Q18	2SA954(L,K)	Ripple filter	FL power supply voltage control (–29V).

2. Set Mode Flowchart

2–1. Outline after POWER ON

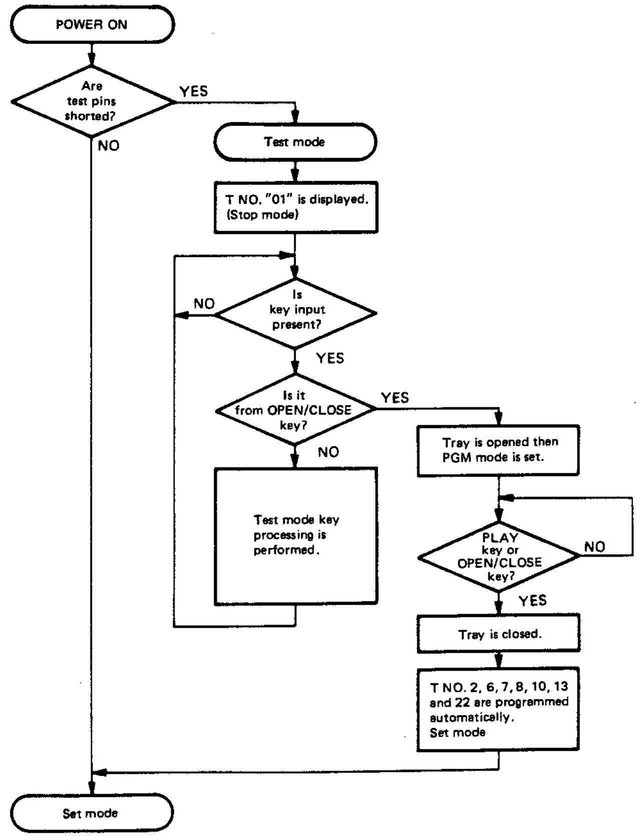


3. Test Mode

3–1. Setting the Test Mode

Unlike previous models, this microprocessor can be put to the test mode by just short-circuiting the test pins even in the set mode (normal condition). (However, the disc must be present in the unit.)

The test mode can also be initiated with the previous method, i. e. by switching the power on with the test pins short-circuited.



CIRCUIT DESCRIPTION

3–2. Key and functions valid in test mode

No.	Input key	Function	Track No. display
1	PLAY	(1) Focusing servo .... ON. (2) Tracking servo .... ON. (3) Feed servo .... ON.	05 ↓ Displayed for a few seconds after completion of (1), (2) and (3). ↓ Disc Track No. is displayed.
2	CHECK	(1) Focusing servo .... ON. (2) Tracking servo .... OFF. (3) Feed servo .... OFF.	03
3	CLEAR	(1) Focusing servo .... ON. (2) Tracking servo .... ON. (3) Feed servo .... OFF.	04
4	STOP	(1) Focusing servo .... OFF. (2) Tracking servo .... OFF. (3) Feed servo .... OFF.	01
5	REPEAT	(1) Tray .... Opened. (2) Laser .... ON. The REPEAT function is canceled when the tray is closed by pressing the tray. The Track No. display 01.	02
6	▶▶	In the STOP mode, moves the pickup slightly toward the outer position of disc. When feed servo is ON, sets the track gain to "H".	
7	◀◀	In the STOP mode, moves the pickup slightly toward the inner position of disc. When feed servo is ON, sets the track gain to "L".	
8	▶▶|	Turns all FL display lamps ON.	
9	|◀◀	Turns all FL display lamps OFF.	
10	Numeric key (0 ~ 9)	Jumps tracks as shown below.	

Key	1	2	3	4	5
Number of tracks	1	4	16	32	1000
Direction	Outer				
Key	6	7	8	9	0
Number of tracks	1	4	16	32	1000
Direction	Inner				

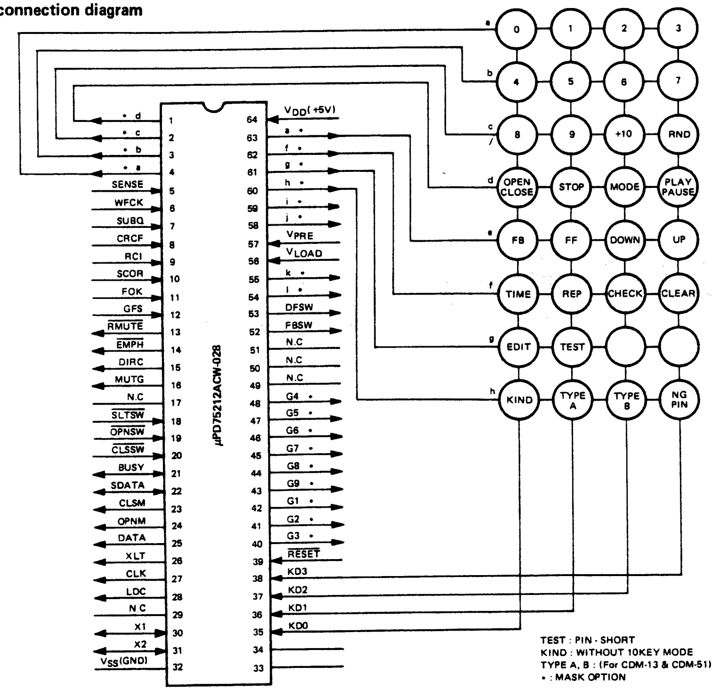
No.	Input key	Function	Track No. display
11	OPEN/CLOSE	When the tray is opened then closed, Track No. 2, 6, 7, 8, 10, 13 and 22 are programmed and the test mode is canceled.	
12	P.MODE	Track No. 2, 6, 7, 8, 10, 13 and 22 are programmed and the test mode is canceled.	

Note : In test mode, characters "TRACK NO." go OFF every time a track key is pressed or a key is pressed for checking PC board wiring.

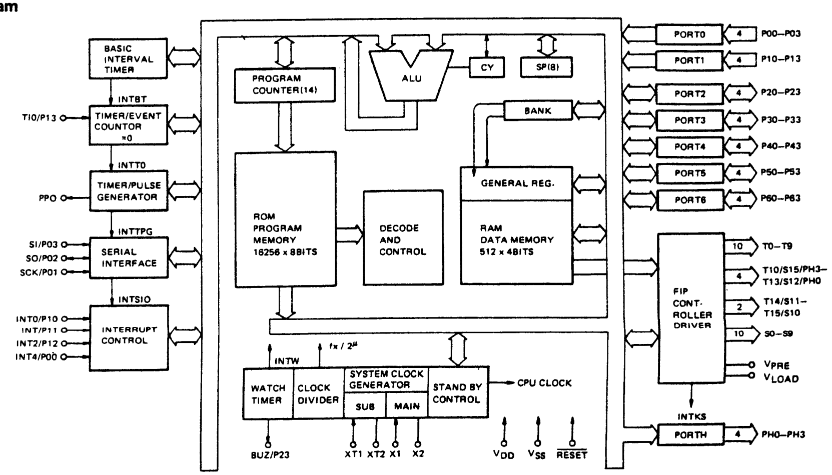
CIRCUIT DESCRIPTION

4. Microprocessor μPD75212ACW-028 (X32-1260-23, X32-1262-73 : IC7) Japan made (X32-1302-72 : IC7) Singapore made

4–1. Terminal connection diagram



4–2. Block diagram



4–3. Terminal description

Terminal No.	Terminal Name	I/O	Function Name	Function
1 ~ 4	S3 ~ S0	O	d ~ a	FL segment control terminals (also used for key scan signals).
5	P00/INT4	I	SENSE	Signal detection terminal for SENSE signal from signal processor and servo ICs.
6	P01/$\overline{\text{SCK}}$	I	WFCK	Q data read clock input terminal.
7	P02/SO	I	SUBQ	Q data input terminal.
8	P03/SI	I	CRCF	Q data CRC check result input terminal. ("H" : OK)
9	P10/INT0	I	RCI	Remote control input terminal.
10	P11/INT1	I	SCOR	Sub-code frame sync detection signal input terminal.
11	P12/INT2	I	FOK	Input terminal for FOK signal from RF amp.
12	P13/TIO	I	GFS	Frame sync signal input terminal. ("H" : Frame sync)
13	P20	O	$\overline{\text{RMUTE}}$	Analog muting control terminal. (Active "L")
14	P21	O	$\overline{\text{EMPH}}$	Deemphasis control terminal. (Active "H")
15	P22	O	DIRC	DIRC terminal of servo IC.
16	P23	O	MUTG	MUTE terminal of signal processor IC. (Active "H")
17	P30	–	–	Not used.
18	P31	I	$\overline{\text{SLTSW}}$	Sled limit switch. (Innermost position : "L")
19	P32	I	$\overline{\text{OPNSW}}$	Tray open switch. (Open : "L")
20	P33	I	$\overline{\text{CLSSW}}$	Tray close switch. (Close : "L")
21	P60	I/O	BUSY	Serial BUSY signal input/output terminal.
22	P61	I/O	SDATA	Serial DATA signal input/output terminal.
23	P62	O	CLSM	Tray motor close terminal.
24	P63	O	OPNM	Tray motor open terminal.
25	P40	O	DATA	Signal processor and servo IC control output terminal.
26	P41	O	XLT	Signal processor and servo IC control output terminal.
27	P42	O	CLK	Signal processor and serco IC control output terminal.
28	P43	O	LDC	Laser ON/OFF signal output terminal. (Active "L")
29	PPO	–	–	Not used.
30, 31	X1, X2	I/O	X1, X2	System clock input/output terminals.
32	VSS	–	VSS	GND.
33, 34	XT1, XT2	–	–	Not used.
35 ~ 38	P50 ~ P53	I	KD0 ~ KD3	Input terminals for key return signals from key matrix.
39	RESET	I	$\overline{\text{RESET}}$	Reset input terminal. (Active "L")
40 ~ 48	T0 ~ T8	O	G9 ~ G1	FL digit control terminals.
49 ~ 51	T9 ~ T11	–	–	Not used.
52	S13	O	FBSW	Focusing bias switch. (Active "L")
53	S12	O	DFSW	Defect switch. (Active "H")
54, 55	S11, S10	O	l, k	FL segment control terminals.
56	VLOAD	I	VLOAD	FL driver negative power supply. (–30V)
57	VPRE	I	VPRE	FL predriver power supply.
58 ~ 63	S9 ~ S4	O	j ~ e	FL segment control terminals. (Also used for key-scan signals)
64	VDD	I	VDD	Power supply. (+5V)

DP-720

CIRCUIT DESCRIPTION

5. RF AMP CXA1081M (X29-1890-02 : IC1) Japan made (X29-1890-03 : IC1) Singapore made

General

The CXA1081M is an IC developed for use in Compact Disc players. It incorporates a 3-spot optical pickup RF output amplifier, a focusing error amplifier, a tracking error amplifier, and other signal processing circuitry, such as focus OK, mirror, defect, and EFM comparator circuits, as well as a laser diode APC (Automatic Power Control) circuit.

Features

- Operates on a signal +5 V power supply, as well as on a ±5 V dual-voltage power supply.
- Low power consumption (100 mW with ±5 V, 50 mW with +5 V).
- An APC circuit which accepts either a P-sub or N-sub laser diode.
- A minimum of external parts required.
- A disc defect detector circuit for improved playability.

Structure

Bipolar silicon monolithic IC

Functions

- RF amplifier
- Focus OK detector circuit
- Mirror detector circuit
- Tracking error amplifier
- Defect detector circuit
- APC circuit
- EFM comparator
- Auto asymmetry control amplifier

5–1. Block diagram

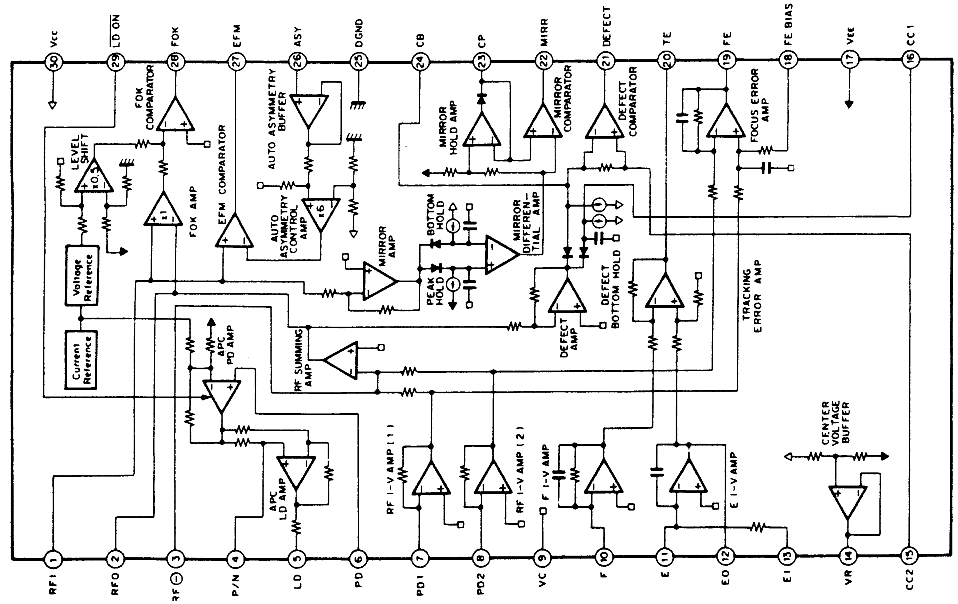


Fig. 5–1

CIRCUIT DESCRIPTION

5–2. Explanation of terminals (V_{CC}= 2.5V, V_{EE}= D_{GND}= –2.5V, VC= GND)

Terminal No.	Terminal name	I/O	DC voltage (V)	Function
1	RFI	I	0	Input pin for the C-coupled signal output from the RF summing amplifier.
2	RFO	O	V_{RFO}	RF summing amplifier output pin. Used as the check point for the eye pattern.
3	RF⊖	I	0	RF summing amplifier feedback input pin.
4	P/N	I	0 (VC)	P-sub/N-sub select pin for the LD (Laser Diode). (DC voltage: in N-sub mode)
5	LD	O	–1.8	*APC LD amplifier output pin. (DC voltage: PD open in N-sub mode)
6	PD	I	0	*APC LD amplifier input pin. (DC voltage: open)
7	PD1	I	0	RF I-V amplifier (1) inverted input pin. Current input by connecting to the photodiode A + C terminal.
8	PD2	I	0	RF I-V amplifier (2) inverted input pin. Current input by connecting to the photodiode B + D terminal.
9	VC	–	0	Connected to GND when using a positive (+)/negative (–) dual-voltage power supply. Connected to VR (pin 14) when using a single-voltage power supply.
10	F	I	0	F I-V amplifier inverted input pin. Current input by connecting to the photodiode F terminal.
11	E	I	0	E I-V amplifier inverted input pin. Current input by connecting to the photodiode E terminal.
12	EO	O	0	E I-V amplifier output pin.
13	EI	I	0	E I-V amplifier feedback input pin. For E I-V amplifier gain adjustment.
14	VR	O	V_{CVO}	DC voltage output pin of $(V_{CC} + V_{EE})/2$.
15	CC2	I	1.0	Input pin for the C-coupled signal output from the defect bottom hold.
16	CC1	O	1.2	Defect bottom hold output pin.
17	V_{EE}	–	–2.5	Connected to the negative power supply when using a positive (+)/negative (–) dual-voltage power supply. Connected to GND when using a single-voltage power supply.
18	FE BIAS	I	0	Bias pin on the focus error amplifier non-inverted side For CMR adjustment of the focus error amplifier.
19	FE	O	V_{FEO}	Focus error amplifier output pin.
20	TE	O	V_{TEO}	Tracking error amplifier output pin.
21	DEFECT	O	V_{DFCTL}	Defect comparator output pin. (DC voltage: connected to a 10 k-ohm load).
22	MIRR	O	V_{MIRL}	Mirror comparator output pin. (DC voltage: connected to a 10 k-ohm load).
23	CP	I	–1.3	Mirror hold capacitor output pin. Mirror comparator non-inverted input.
24	CB	I	0	Defect bottom hold capacitor connect pin.
25	DGND	–	–2.5	Connected to GND when using a positive (+)/negative (–) dual-voltage power supply. Connected to GND (V_{EE}) when using a single-voltage power supply.
26	ASY	I	–	Auto asymmetry control input pin.
27	EFM	O	V_{EFMH}	EFM comparator output pin. (DC voltage: connected to a 10 k-ohm load).
28	FOK	O	V_{FOKL}	FOK comparator output pin. (DC voltage: connected to a 10 k-ohm load).
29	LD ON	I	–2.5 (DGND)	LD ON/OFF select pin. (DC voltage: when LD ON)
30	V_{CC}	–	2.5	Positive power supply.

*APC: Automatic Power Control

Table 5–1

CIRCUIT DESCRIPTION

5–3. Function explanation

● RF amplifier

The photodiode current input to the input pins (PD1, PD2) is converted to a voltage by an equivalent resistance of 58 k-ohms in RF I-V amplifier (1) and (2) respectively.

The voltage which is converted from the current of the photodiode (A + B + C + D) is added in the RF summing amplifier and is output from the RFO pin. The eye pattern can be checked at this pin.

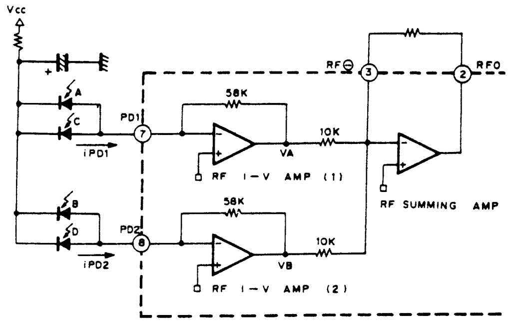


Fig. 5–2 RF I-V AMPLIFIER

The low frequency component of the RFO output voltage, V_{RFO}, is represented by the following equation:

$$V_{RFO} = 2.2 \times (V_A + V_B)$$
$$= 127.6 \text{ k-ohms} \times (i_{PD1} + i_{PD2})$$

● Focus error amplifier

The difference between the RF I-V amplifier (1) output (VA) and the RF I-V amplifier (2) output (VB) is calculated, and the current of the photodiode (A + C – B – D) is converted to a voltage and output.

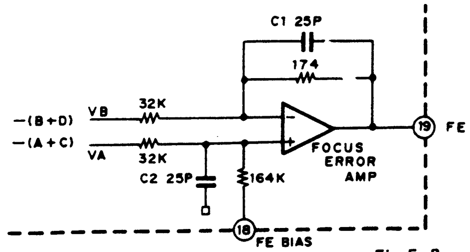


Fig. 5–3

The FE output voltage (low frequency) is represented by the following equation:

$$V_{FE} = 5.4 \times (V_A - V_B)$$
$$= (i_{PD2} - i_{PD1}) \times 315.4 \text{ k-ohms}$$

The common mode rejection ratio of the VR connected to pin ⑱ is maximized when the composite impedance to GND is around 10 k-ohms (with a VR resistance of around 40 k-ohms).

CIRCUIT DESCRIPTION

- **Tracking error amplifier**

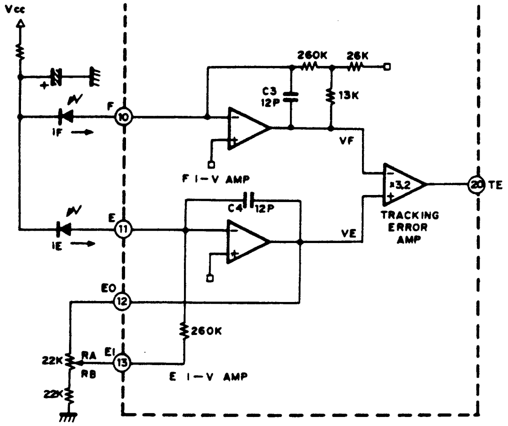


Fig. 5–4

The current from the side spot photodiodes is input to pins E and F and is converted to a voltage by the E I-V amplifier and F I-V amplifier respectively.
That is:

$V_F = iF \times 403$ k-ohms

$V_E = iE \times 260$ k-ohms $\times R_A/(R_B + 22\text{ k}) + (R_A + 260\text{ k})$

The difference between the E I-V amplifier and the F I-V amplifier is calculated by the tracking error amplifier, and the photodiode (E-F) current is converted to a voltage and output.

$V_{TE} = (V_E - V_F) \times 3.2$

$= (iE - iF) \times 1290$ k-ohms

- **Focus OK circuit**

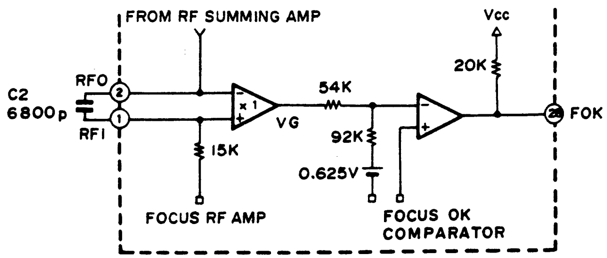


Fig. 5–5

The focus OK circuit creates a timing window, turning the focusing servo ON with the focus search status.
While an RF signal is present at pin ②, an HPF output is present at pin ①. At the same time, the LPF output (opposite phase) of the focus OK amplifier is obtained.
The focus OK output is inverted when $V_{RFI} - V_{RFO}$ is almost equal to −0.37 V.

C2 is used to determine the time constants of the EFM comparator, the HPF in the mirror circuit, and the LPF in the focus OK amplifier. Normally, C2 = 6800pF is selected, with fc = 1kHz. This will prevent degradation of the block error rate due to an RF envelope lack caused by cracks, etc. on the disc.

CIRCUIT DESCRIPTION

- **Mirror circuit**

In the mirror circuit, after the RFI signal is amplified, both its peak and bottom are held.

While the peak hold is held by a time constant which can follow a traverse of 30 kHz, the bottom hold is held by a time constant which can follow a cyclic period envelope variation.

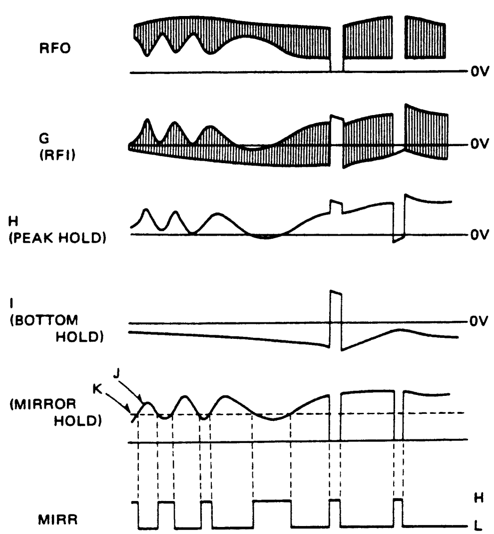


Fig. 5–6

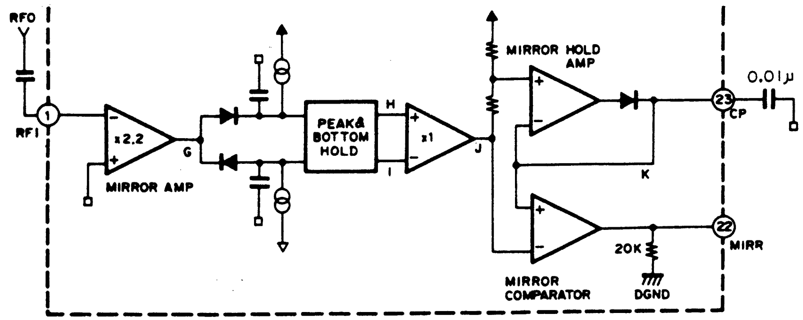


Fig. 5–7

These peak and bottom hold signals, H and I are differentially amplified to obtain the DC-reproduced envelope signal J. This signal is compared with signal K, which is obtained by a peak hold with a large time constant corresponding to 2/3 of the peak value, so that the mirror output is obtained. That is, the mirror output goes "L" on the disc tracks and goes "H" between tracks (mirror section). In addition, the output goes "H" when a defect is detected. The time constant of the mirror hold should be quite large when compared with the traverse signal.

CIRCUIT DESCRIPTION

• EFM comparator

The EFM comparator converts the RF signal into a binary coded signal. Since asymmetry caused by dispersion when manufacturing the discs cannot be reduced by AC coupling only, the reference voltage of the EFM comparator is controlled using the characteristic that the present probability of a 1 or 0 is 50% for the binary coded EFM signal.

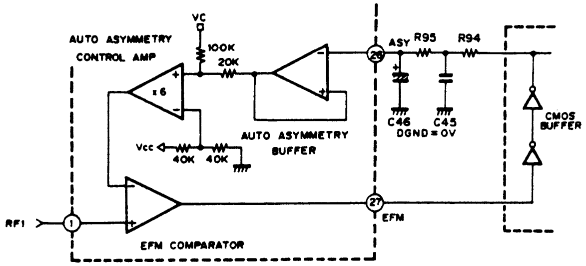


Fig. 5–8

The EFM comparator is designed as a current switching type, and the "H" and "L" levels are not equal to the power voltages. Therefore, feedback is required via a CMOS buffer. R94, R95, C45 and C46 constitute an LPF to obtain the DC component of (Vcc + DGND)/2 (V). If the cut-off frequency (fc) is set to more than 500Hz, leakage of the EFM low frequency signals will be greatly increased and will result in a degradation of the block error rate.

• Defect circuit

After inverting the RFI signal, the defect circuit bottom holds with two long/short time constants. The bottom hold with a shorter time constant responds to a mirror defect of more than 0.1 msec on the disc, and the bottom hold with a longer time constant holds the mirror level obtained immediately before the defective section. These signals are C-coupled, then differentiated with level shifting. The signals are compared with each other to generate the mirror defect detecting signals.

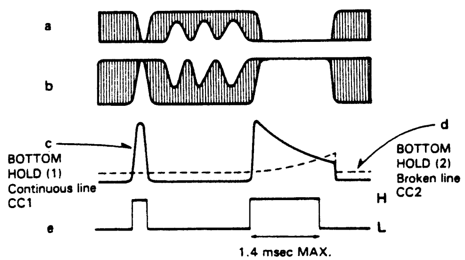


Fig. 5–9

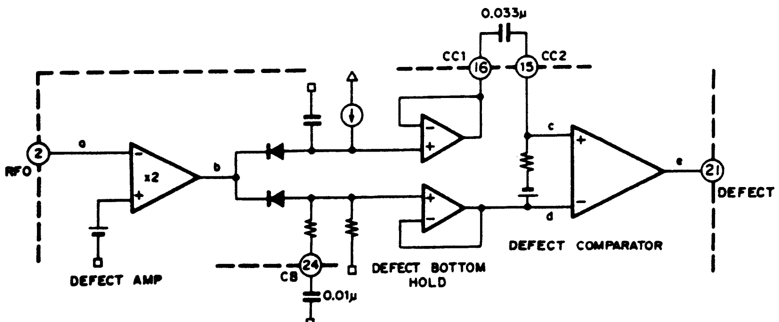


Fig. 5–10

CIRCUIT DESCRIPTION

6. Servo control CXA1244S (X32-1260-23, X32-1262-73 : IC2) Japan made (X32-1302-72 : IC2) Singapore made

CXA1244S is a bipolar IC developed for servo of compact disc (CD) players, and it provides the following functions.

- ○Focus control (search ON/OFF, gain control)
- ○Tracking control (servo ON/OFF, single track jump, multiple track jump, gain control, phase compensation control, brake circuit)
- ○ Sled control (servo ON/OFF, fast forward, fast reverse)

Servo function of each of focus, tracking and sled as well as random access operation are realized through control by microcomputer. Furthermore, the serial data bus can be shared with CX23035.

6–1. Terminal connection diagram

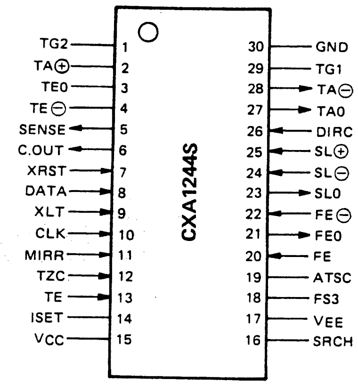


Fig. 6–1

6–2. Block diagram

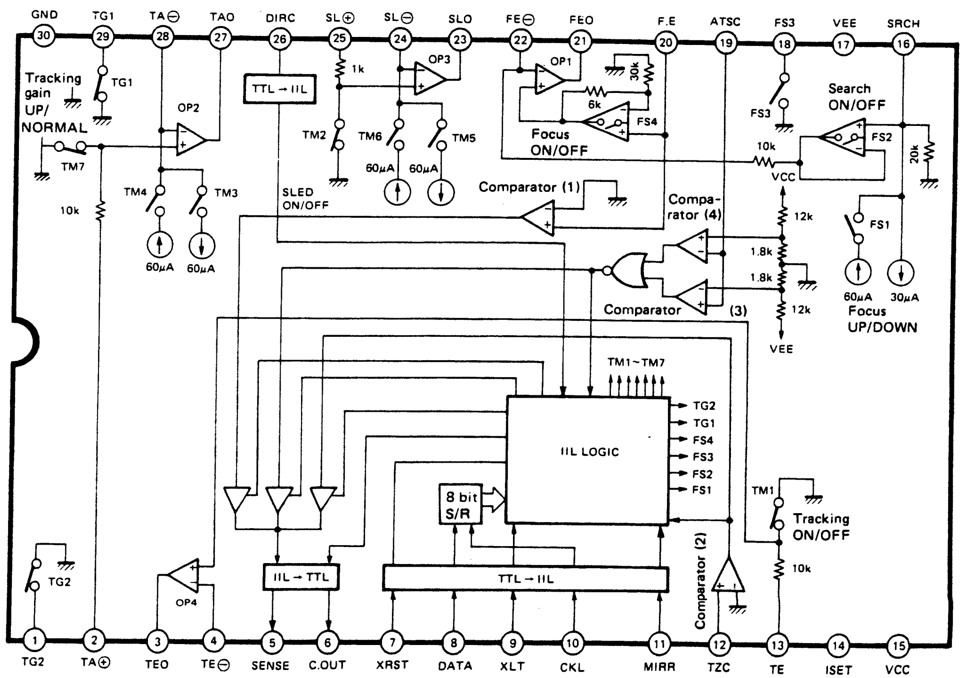


Fig. 6–2

CIRCUIT DESCRIPTION

6–3. Explanation of terminals

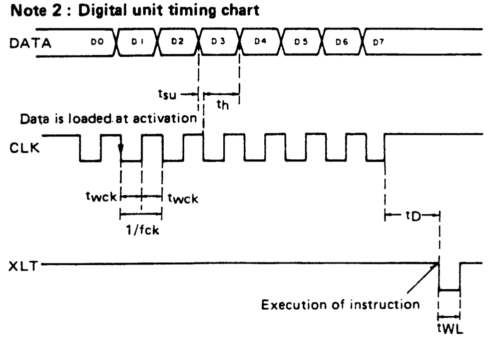
Terminal No.	Terminal name	I/O	Functions
1	TG2		Tracking amplifier gain switching terminal. GND level.
2	TA ⊕		Non-inverted input of operational amplifier 2.
3	TEO		Output of operational amplifier 4.
4	TE ⊖	O	Inverted input of operational amplifier 4.
5	SENSE	O	Output of SSP internal status that corresponds to ADDRESS of CPU → SSP. (Changes in accordance with ADDRESS content of internal serial register.) See Note 1.
6	C. OUT	O	Signal output for counting number of tracks at the time of high speed access.
7	XRST	I	All internal registers are cleared when CPU → SSP "L". Connected with CPU RESET. See Note 2.
8	DATA	I	Serial data transmission of CPU → SSP. Input is made from LSB. D0~D7.
9	XLT	I	Latch of serial data of CPU → SSP. (The contents of internal serial register are transmitted to each address decoded latch.) Transmission at "L". Change to "H" occurs immediately after execution because no edge trigger is produced.
10	CLK	I	CPU → SSP serial data transmission block. Data is read at falling. "H" level before and after transmission.
11	MIRR	I	Mirror signal input from RF amplifier.
12	TZC	I	Tracking error signal is input with C couple. The time constant is determined by one single track jump, but it is usually around 2kHz.
13	TE	I	Tracking error signal input.
14	ISET		Setting of current level for determining focus search voltage, tracking jump voltage and thread feed voltage.
15	Vcc		Power supply terminal. Normally –5V.
16	SRCH		The condenser for determining the time constant of charge/discharge waveform for focus search is connected.
17	VEE		Power supply terminal. Normally –5V.
18	FS3		Focus amplifier gain switching terminal. GND level.
19	ATSC		Such information that a mechanical shock was applied to the player is input. Simply, a trakcing error is input through BPF.
20	FE	I	Input of focus error signal.
21	FEO	O	Output of operational amplifier 1.
22	FE ⊖	I	Inverted input of operational amplifier 1.
23	SLO	O	Output of operational output 3.
24	SL ⊖	I	Inverted input of operational amplifier 3.
25	SL ⊕	I	Non-inverted input of operational amplifier 3.
26	DIRC	I	Used at the time of one track jump. Normally "H". The direction of the track jump pulse is reversed with "L". Setting is made in the normal tracking mode by changing to "H". "L" for a fixed length of time with detection of activation, deactivation of TZC.
27	TAO	O	Output of operational amplifier 2.
28	TA ⊖	O	Inverted input of operational amplifier 2.
29	TG1		Tracking amplifier gain switching terminal. GND level.
30	GND		GND terminal of IC.

Table 6–1

Note 1 : SENSE terminal output

Serial data upper 4 bits	ADDRESS content	SENSE terminal output	Explanation
0 0 0 0	FOCUS CONTROL	FZC	"H" when focus zero cross, Focus erro voltage is 0V or higher. Used at the time of FOCUS PULL operation.
0 0 0 1	TRACKING CONTROL	AS	"H" when the ATSC input level exceeds the wind comparator level (VTH = ±Vcc x 13%). But this is not used in this equipment.
0 0 1 0	TRACKING MODE	TZC	Judgement output of positive or negative of tracking zero cross, tracking error. When used at the time of single track jump, DIRC is reduced to "L" on detection of TZC ↑, in FWD JUMP or on detection of TZC ↓ in REV JUMP.

Note 2 : Digital unit timing chart



DP-720

CIRCUIT DESCRIPTION

6–4. System control

COMMAND	ADDRESS				DATA				SENSE
	D7	D6	D5	D4	D3	D2	D1	D0	
FOCUS CONTROL	0	0	0	0	FS4 FOCUS ON	FS3 GAIN DOWN	FS2 SEARCH ON	FS1 SEARCH UP	FZC
TRACKING CONTROL	0	0	0	1	ANTI SHOCK	BREAK ON	TG2 GAIN	TG1* SET	AS
TRACKING MODE	0	0	1	0	TRACKING* MODE		SLED* MODE		TZC

Table 6–2

GAIN SET* TG1, TG2 may be set independently.
In the case of ANTI SHOCK = 1 (00011XXX), both TG1, TG2 are inverted when ANTI SCHOCK = "H".

SLED MODE *

	D1	D0
OFF	0	0
SERVO ON	0	1
FWD MOVE	1	0
REV MOVE	1	1

TRACKING MODE *

	D3	D2
OFF	0	0
SERVO ON	0	1
FWD JUMP	1	0
REV JUMP	1	1

CIRCUIT DESCRIPTION

6–5. Serial data truth value table.

Serial data	Hexa-decimal	Function
FOCUS CONTROL		FS = 4321
00000000	S00	0000
00000001	S01	0001
00000010	S02	0010
00000011	S03	0011
00000100	S04	0100
00000101	S05	0101
00000110	S06	0110
00000111	S07	0111
00001000	S08	1000
00001001	S09	1001
00001010	S0A	1010
00001011	S0B	1011
00001100	S0C	1100
00001101	S0D	1101
00001110	S0E	1110
00001111	S0F	1111

Table 6–3

TRACKING CONTROL		D2	AS = 0 TG = 2 1	AS = 1 TG = 2 1
00010000	S10	0	0 0	0 0
00010001	S11	0	0 1	0 1
00010010	S12	0	1 0	1 0
00010011	S13	0	1 1	1 1
00010100	S14	1	0 0	0 0
00010101	S15	1	0 1	0 1
00010110	S16	1	1 0	1 0
00010111	S17	1	1 1	1 1
00011000	S18	0	0 0	1 1
00011001	S19	0	0 1	1 0
00011010	S1A	0	1 0	0 1
00011011	S1B	0	1 1	0 0
00011100	S1C	1	0 0	1 1
00011101	S1D	1	0 1	1 0
00011110	S1E	1	1 0	0 1
00011111	S1F	1	1 1	0 0

Table 6–4

TRACKING MODE		DC = 1 TM = 654321	DC = 1 654321	DC = 1 654321
00100000	S20	000000	001000	000011
00100001	S21	000010	001010	000011
00100010	S22	010000	011000	100001
00100011	S23	100000	101000	100001
00100100	S24	000001	000100	000011
00100101	S25	000011	000110	000011
00100110	S26	010001	010100	100001
00100111	S27	100001	100100	100001
00101000	S28	000100	001000	000001
00101001	S29	000110	001010	000011
00101010	S2A	010100	011000	100001
00101011	S2B	100100	101000	100001
00101100	S2C	001000	000100	000011
00101101	S2D	001010	000110	000011
00101110	S2E	011000	010100	100001
00101111	S2F	101000	100100	100001

Table 6–5

DC : DIRC input terminal

DP-720

CIRCUIT DESCRIPTION

6–6. Explanation of functions

The input data for causing this IC to operate is composed of 8 bits. It is hereinafter expressed in two hexadecimal digits like $XX. (X is 0~F.)

Instructions to CXA1244S are generally divided into three types, i.e., $0X, $1X and $2X. Standard methods for use of these three types are explained below.

• $0X (⑤ SENSE is "FZC")

This instruction is related to control of focus servo, and its bit composition is as follows.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	FS4	FS3	FS2	FS1

Four switches, i.e., FS1~FS4, are what are related to focus, and they correspond to D0~D3 respectively.

1) FS1, FS2 and focus search

The operation of FS1, FS2 is described next. ㉑, ㉒ etc. in Fig. 6–3 indicate terminal numbers of CXA1244S (same hereinafter) OP1 is the operational amplifier for focus servo and the output of FS2 is connected to its inversion terminal. FS2 is such a switch that is ON and works as a usual voltage follower at the time of 1; and that its output is of high impedance at the time of 0. FS1 is a simple current switch which is OFF at the time of 1 and works to allow flow of 60μA at the time of 0. This value of 60μA is what is obtained when 240μA is fed to ISET ⑭ terminal. The voltage for focus search is produced using these FS1, FS2.

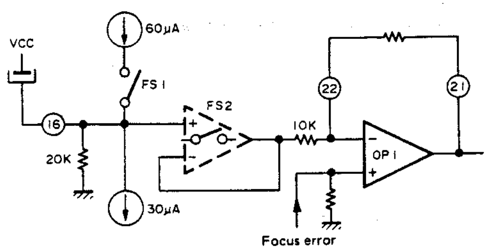


Fig. 6–3 Explanation of FS1, FS2

I $00 ⑯ terminal is charged to (60μA−30μA) x 20kΩ = 0.6V when FS1 = 0. Further, because FS2 = 0, This voltage is not transmitted thereafter, and ouput ㉑ terminal is of 0V.

II $02 FS2 only becomes 1 from the status described above. The output of FS2 is + 0.6V at this time and a negative output is directed to op2. This voltage level is specified as follows.

$$\underbrace{(60\mu A-30\mu A)}_{\text{At the time of } 240\mu A\ (⑭)} \times 20k\Omega \times \frac{\text{Resistance value between ㉑ − ㉒}}{10k\Omega} \quad \ldots\ldots \text{Expression (1)}$$

III $03 FS1 becomes 1 from the status described above and the current source of + 60μA is disconnected. Then, the CR's charge/discharge circuit is formed and the voltage at ⑯ terminal decreases as the time elapses as shown in Fig. 6–4.

This time constant is specified by internal 20kΩ and external condenser C101 22μF.

It is possible to produce the focus serach voltage by alternately instructing these II and III. (Fig. 6–5)

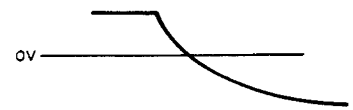


Fig. 6–4 Voltage at ⑯ terminal when FS1 = 0 → 1

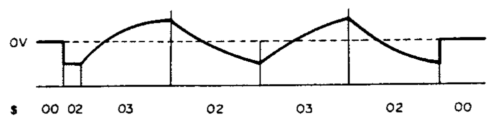


Fig. 6–5 Search voltage is produced by $02 ⇌ $03 (voltage at ⑯ terminal)

CIRCUIT DESCRIPTION

2) Explanation of FS4

This switch is a voltage follower (but the gain is 1.2 times) at the time of 1 and the output is open at the time of 0, like FS2 described earlier. This switch bears focus servo ON/OFF as located between focus error input 20 and input of OP1 described earlier.

$00 → $08

Focus OFF ← Focus ON

3) Focusing procedure

The polarity is specified as follows for explanation.

- The lens searches in the direction of far → near to the disc.
- Output voltage ㉑ changes as negative → positive at this time.
- Further, the S curve of focus changes as shown in Fig. 6–6.

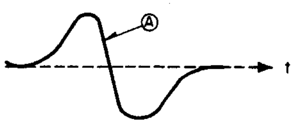


Fig. 6–6 S curve

Focus servo is applied with point Ⓐ shown in Fig. 6–6 as the actuation point. In general, the time when focus search is made and the focus servo switch is ON during passage through point Ⓐ. Furthermore, ANDing is made with focus OK signal (FOK) in order to prevent malopera-tion.

This IC is of such a design that what is obtained by comparing the focus error with 0V is output out of SENSE ⑤ terminal as the signal passing through point Ⓐ and is named as FZC (Focus Zero Cross).

Focus OK means a signal that indicates that focus is applied (may be applied, in this case), and it is output out of ㉘ terminal of head amplifier IC1 (CXA1081M) in X29-1890-XX.

when the above description is summarized, focus is applied in accordance with a tim chart like what is shown in Fig. 6–7.

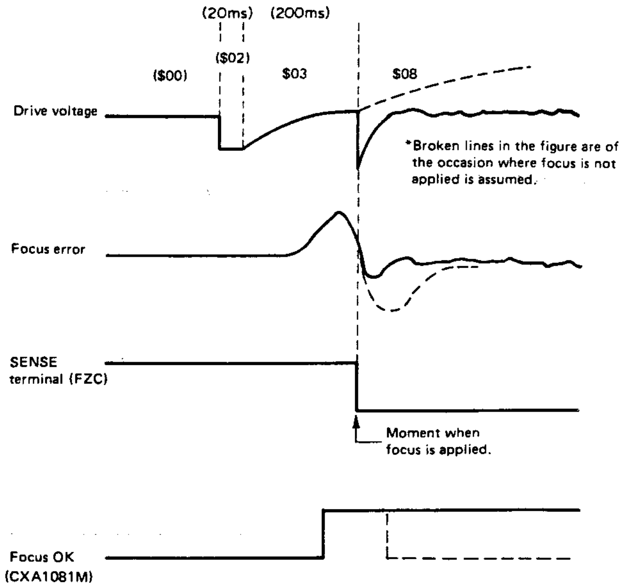


Fig. 6–7 Timing chart of focus OK

CIRCUIT DESCRIPTION

4) SENSE ⑤ terminal

As the output type is open collector of an NPN transis-tor, it is used with 22kΩ pull up. What is output varies by the input data. That is;

- FZC with $0X
- "H" when the absolute value of the voltage applied to AS terminal exceeds 0.65V, or "L" when it is up to 0.65V, with $1X.
- TZC with $2X

5) FS3 switch

The type of this switch as shown in Fig. 6–8. It is of GND when FS3 is 1 or is of high impedance when FS3 is 0. See "Method for use of FS3" in the explanation of circuit operation.

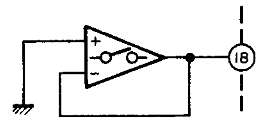


Fig. 6–8 FS3

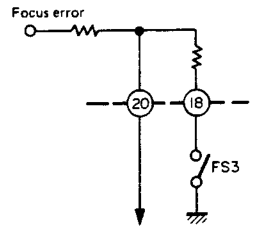


Fig. 6–9 Typical use of FS3

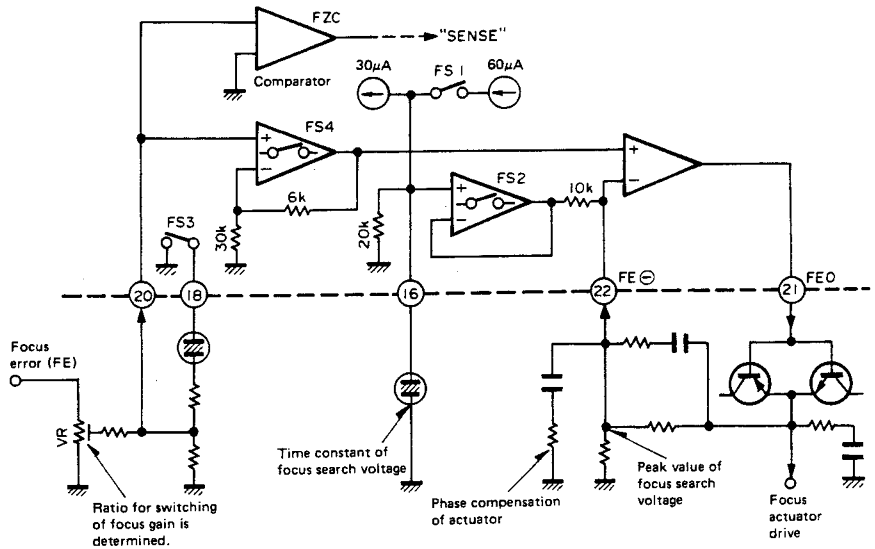


Fig. 6–10

CIRCUIT DESCRIPTION

• $1X (⑤ SENSE is "AS")

This instruction is related to TG1, TG2 and brake circuit ON/OFF. The bit composition is as follows.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1		Brake circuit ON/OFF	TG2	TG1

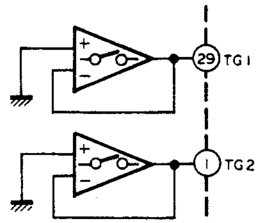


Fig. 6–11 TG1, TG2

1) TG1, TG2

The circuit type of these switches is same as that of FS3 shown in Fig. 6–8. However, the logic is opposite. High impedance is obtained with 1, and GND level is obtained with 0. The purpose of the switch is switching between UP/NORMAL of the tracking servo gain. One switch is used for switching of the gain and another for switching of the phase. A typical circuit is shown in Fig. 6–12.

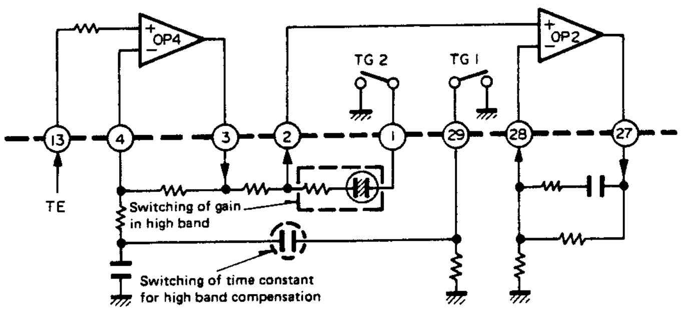


Fig. 6–12 Typical use of TG1, TG2

CIRCUIT DESCRIPTION

2) Brake circuit

The brake circuit is OFF (TM7 is open) when D2 = 0.

The brake circuit is ON (TM7 is open) when D2 = 1.

The brake circuit is explained next. See the section of 100 track jump and 10 track jump as for when the brake circuit is used.

The brake circuit is provided for preventing occurrence of such a phanomenon that only 10 tracks were jumped, even if it was intended to jump 100 tracks, due to the fact that setting of the actuator is exteremely inferior because the servo circuit exceeds the linear range after 100 track jump or 10 track jump. The phase relation between RF's envelope and tracking error is deviated by 180 degrees between the case where the actuator runs across tracks in the radial direction outward and the case where the same runs inward. The unnecessary portion of the tracking error is cut and brake is applied by making use of this nature, for improving setting of the actuator after track jump.

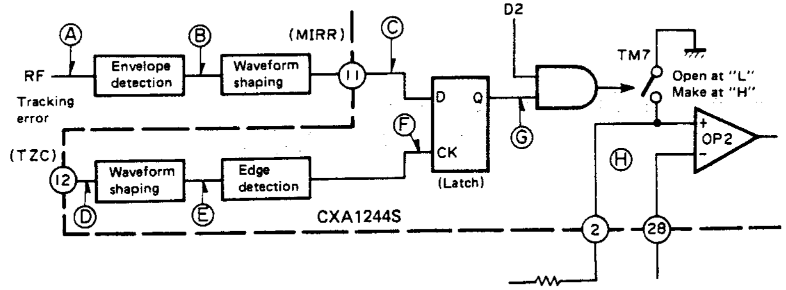


Fig. 6–13 Motion of TM7 (brake circuit)

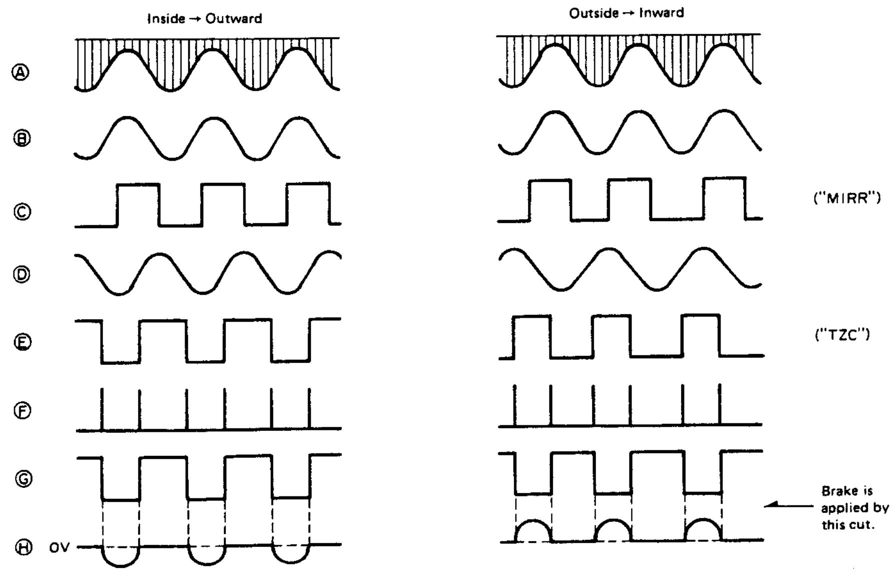


Fig. 6–14 Explanation of Fig. 6–13 (external waveform)

CIRCUIT DESCRIPTION

- **$2X (⑤ SENSE is "TZC")**

This instruction is related to production of jump pulse and fast feed pulse at the time of ON/OFF of tracking servo and sled servo and also at the time of access.

D7	D6	D5	D4	D3 D2	D1 D0
0	0	1	0	Tracking control 00 : OFF 01 : Servo ON 10 : F-jump 11 : R-jump ⇩ TM1, TM3, TM4	Sled control 00 : OFF 01 : Servo ON 10 : F-Fast feed 11 : R-Fast feed ⇩ TM2, TM5, TM6

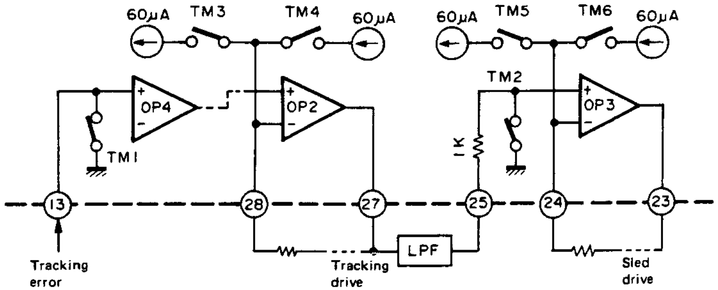


Fig. 6–15 TM1 ~ TM7

The circuit composition is shown in Fig. 6–15. TM1, TM2 make servo ON/OFF, and TM3~TM6 produce jump pulse and fast feed pulse. See truth value table for details.

Figure 60μA is observed in Fig. 6–15. This value is of the case where 240μA is fed to ISET ⑭ terminal like SF1. The circuit of ⑭ terminal is as shown in Fig. 6–16. Therefore, the potential is around (–)VEE + 0.9V.

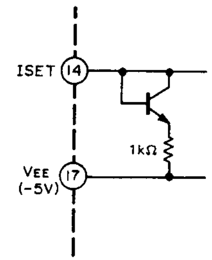


Fig. 6–16 ISET terminal

1) DIRC ㉖ terminal and single track jump

1 track jump usually gives an acceleration pulse, and then observes the tracking error; gives deceleration pulses for a fixed length of time from the time when the tracking error ran across 0 point, and again turns ON the tracking servo. 100 track jump to be explained in the next paragraph is satisfactory if approximately 100 tracks are jumped, but 1 track jump should be absolutely 1 track jump. Therefore, such a complicated measure is taken.

Therefore, DIRC (Direct Control) terminal is provided for this IC in order to facilitate single track jump by its operation. That is, for performing single track jump using DIRC (DIRC is usually "H")

- ○An acceleration pulse is produced. ($2C if REV; or $28 if FWD)
- ○DIRC is changed to "L" by TZC ↓ (or TZC ↑). (⑤ SENSE is "TZC".) The polarity of the jump pulse is inverted and deceleration is applied.
- ○DIRC is changed to "H" after a fixed length of time. Both tracking servo and sled servo are ON automatically.

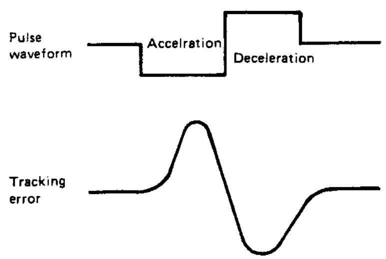


Fig. 6–17 Pulse waveform and tracking error of signal track jump

CIRCUIT DESCRIPTION

2) 100 track jump

With this IC, basically it is not possible to change the amplitude of the jump pulse between 1 track jump and 100 track jump. (Because the value of the current input to ISET ⑭ terminal is fixed.)

Therefore, the amplitude is determined by 1 track jump and 100 track jump is controlled by time with the voltage remaining unchanged.

100 track jump is of smooth feed by jointly using sled fast feed (so-called "kick-off") besides drive of the tracking actuator. The length of this kick off is determined so that the access time is the minimum.

Brake circuit ON and tracking gain UP are made to stabilize the setting operation after the jump.

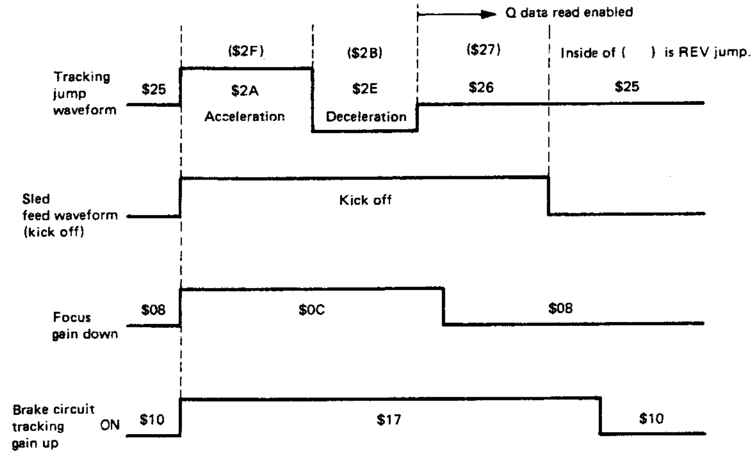


Fig. 6–18 100 track jump timing chart

3) 10 track jump

As this is intermediate between 100 and 1, the required number of tracks is set at a value that is close to 10, and therefore, the jump pulse width is determined by counting the number of jumped tracks.

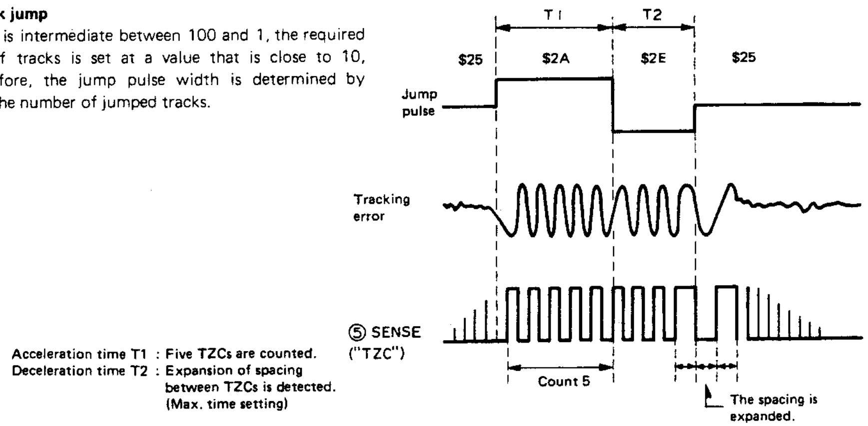


Fig. 6–19 10 track jump

CIRCUIT DESCRIPTION

4) Access by making joint use of 100, 10 and 1 track jumps

Jump pulses and kick off pulses (that is, $2X relaiton) are set as described in the paragraph of $2X and subsequent, and as for $1X relation, instructions are output in a batch.

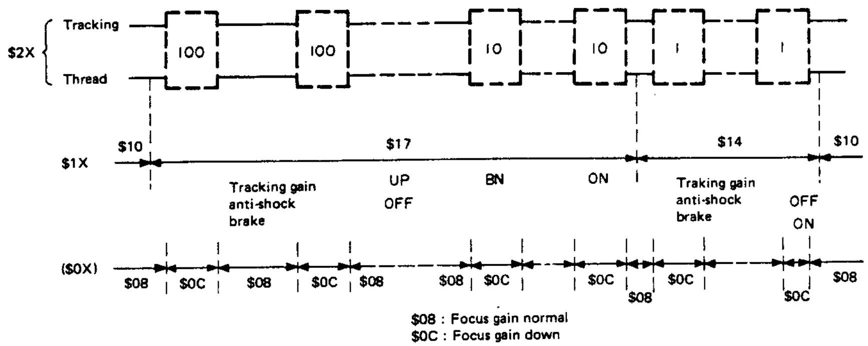


Fig. 6–20 Typical access time instruction codes

- **How to use high speed access and Count Out ⑥**

It is needless to say that access time for head search of a music and so forth is shorter. In the access using 100, 10, 1 track jump, however, about 4 seconds is the limit from the innermost periphery to the outermost periphery of the disc. It is because 100 track jump consumes more than 80% of the time, and it is possible to shorten the time if the length of time of this "major movement" can be shortened. As the distance from the current location to the destination can be learned from the TOC and the absolute time of the current location, rough feed is made for this distance.

Several methods are available as for the means to replace this distance. In general, it is the number of tracks divided by 1.6μm, sled motor revolution (number of steps, if it is a stepping motor) or potentiometer's voltage, if provided.

C.OUT ⑥, which is a terminal exclusive for counting number of tracks is provided on this IC in order to make correspondence to counting of number of tracks. As this signal is what is obtained by latching MIRROR signal by the edge of TZC (that is, same as the signal used in the brake circuit), and therefore, even if tracking error signal, etc. include noise, such noise is ignored.

CIRCUIT DESCRIPTION

7. Signal processor CXD1135QZ (X32-1260-23, X32-1262-73 : IC4) Japan made (X32-1302-72 : IC4) Singapore made

General

The CXD1135QZ is a digital signal processing LSI for a Compact Disc player, and has the following functions.

1. Bit clock reproduction by an EFM-PLL circuit
2. EFM data demodulation
3. Frame sync signal detection, protection and insertion
4. Powerful error detection and correction
5. Interpolation with an average value, or by holding the previous value
6. Demodulation of a sub code signal, error detection of a sub code Q
7. Spindle motor CLV servo
8. 8-bit tracking counter
9. CPU interface with a serial bus
10. Sub code Q register
11. Digital filter
12. Digital audio interface output

Features

- All digital signals used in playback can be processed using only a single chip.
- An aperture-correction digital filter is built in.

Structure

CMOS IC

7–1. Block diagram

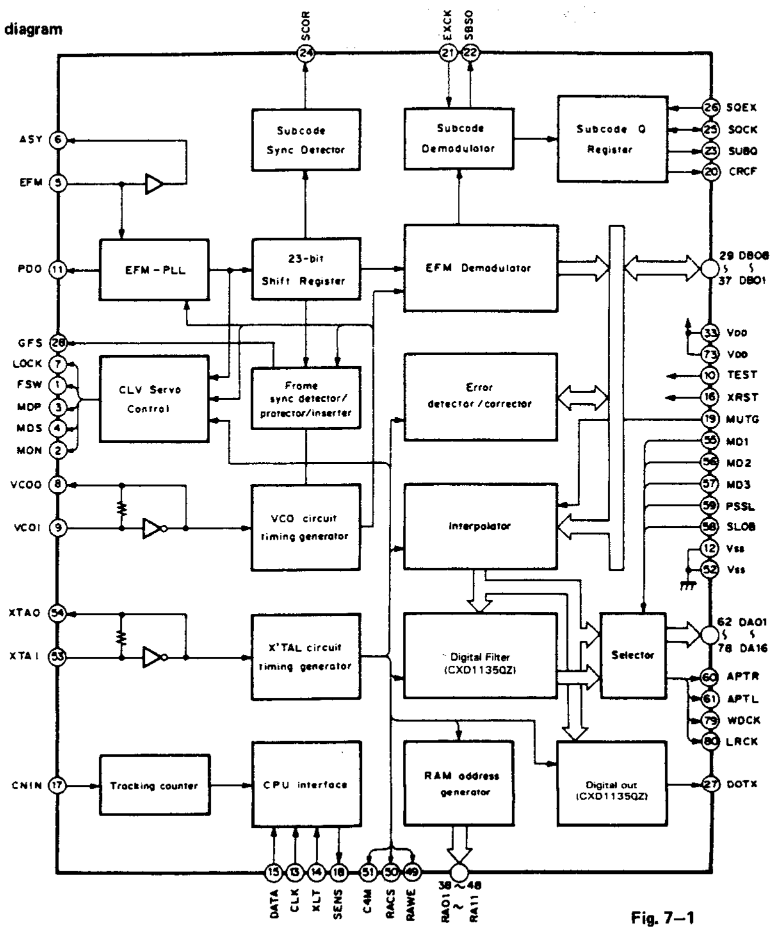


Fig. 7–1

CIRCUIT DESCRIPTION

7-2. Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	FSW	O	Time constant switching output of output filter of spindle motor.
2	MON	O	ON/OFF control output of spindle motor.
3	MDP	O	Drive output of spindle motor. Rough speed control in CLV-S mode and phase control in CLV-P mode.
4	MDS	O	Drive output of spindle motor. Speed control in CLV-P mode.
5	EFM	I	EFM signal input from RF amplifier.
6	ASY	O	Output for controlling the slice level of EFM signal.
7	LOCK	O	Samples the GFS signal with WFCK/16, and outputs "H" when the level is high. When it is "L" for eight times, in arrow, outputs "L".
8	VCOO	O	VCO output. f = 8.6436 MHz when locked to EFM signal.
9	VCOI	I	VCO input.
10	TEST	I	(0 V)
11	PDO	O	Phase comparison output of EFM signal and VCO/2.
12	Vss	—	GND (0 V)
13	CLK	I	Serial data transmission clock input from CPU. Data is latched at rising edge of a clock.
14	XLT	I	Latch input from CPU. Data (serial data from CPU) from the 8 bit shift register is latched in each register.
15	DATA	I	Serial data input from CPU.
16	XRST	I	System reset input. Reset at "L".
17	CNIN	I	Input of tracking pulse.
18	SENS	O	Output of internal status in correspondence to the address.
19	MUTG	I	Muting input. In the case when ATTM of internal register A is "L". Normal status when MUTG is "L" or soundless state when it is "H".
20	CRCF	O	Output of result of CRC check of sub code Q.
21	EXCK	I	Clock input for sub code serial output.
22	SBSO	O	Sub code serial output.
23	SUBQ	O	Sub code Q output.
24	SCOR	O	Sub code sync S0 + S1 output.
25	SQCK	I/O	Sub code Q read-off clock.
26	SQEX	I	SQCK select input.
27	DOTX	O	DIGITAL OUT output. (Outputs the $\overline{\text{WFCK}}$ signal when CXD1130Q or D0 is off)
28	GFS	O	Display output of frame sync lock status.
29	DB08	I/O	Data pin of external RAM. DATA8 (MSB)
30	DB07	I/O	Data pin of external RAM. DATA7
31	DB06	I/O	Data pin of external RAM. DATA6
32	DB05	I/O	Data pin of external RAM. DATA5
33	VDD	—	Power supply (+5 V)
34	DB04	I/O	Data pin of external RAM. DATA4
35	DB03	I/O	Data pin of external RAM. DATA3
36	DB02	I/O	Data pin of external RAM. DATA2
37	DB01	I/O	Data pin of external RAM. DATA1 (LSB)
38	RA01	O	Address output of external RAM. ADDR01 (LSB)
39	RA02	O	Address output of external RAM. ADDR02
40	RA03	O	Address output of external RAM. ADDR03
41	RA04	O	Address output of external RAM. ADDR04
42	RA05	O	Address output of external RAM. ADDR05
43	RA06	O	Address output of external RAM. ADDR06

Table 7-1

CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Function
44	RA07	O	Address output of external RAM. ADDR07
45	RA08	O	Address output of external RAM. ADDR08
46	RA09	O	Address output of external RAM. ADDR09
47	RA10	O	Address output of external RAM. ADDR10
48	RA11	O	Address output of external RAM. ADDR11 (MSB)
49	RAWE	O	Write Enable signal output to external RAM. (Active at "L").
50	RACS	O	Chip select signal output to external RAM. (Active at "L").
51	C4M	O	Crystal dividing output. f = 4.2336 MHz.
52	Vss	—	GND (0 V).
53	XTAI	I	Crystal oscillator input. f = 8.4672 MHz or 16.9344 MHz depending on the mode selected.
54	XTAO	O	Crystal oscillator output. f = 8.4672 MHz or 16.9344 MHz depending on the mode selected.
55	MD1	I	Mode select input 1.
56	MD2	I	Mode select input 2.
57	MD3	I	Mode select input 3.
58	SLOB	I	Audio data output code select input. 2's complement output when "L", offset binary output when "H".
59	PSSL	I	Audio data output mode select input. Serial output when "L", parallel output when "H".
60	APTR	O	Aperture compensation control output. "H" when R-ch.
61	APTL	O	Aperture compensation control output. "H" when L-ch.
62	DA01	O	DA01 (parallel audio data LSB) output when PSSL = "H", C1F1 output when PSSL = "L".
63	DA02	O	DA02 output when PSSL = "H", C1F2 output when PSSL = "L".
64	DA03	O	DA03 output when PSSL = "H", C2F1 output when PSSL = "L".
65	DA04	O	DA04 output when PSSL = "H", C2F2 output when PSSL = "L".
66	DA05	O	DA05 output when PSSL = "H", C2FL output when PSSL = "L".
67	DA06	O	DA06 output when PSSL = "H", C2PO output when PSSL = "L".
68	DA07	O	DA07 output when PSSL = "H", RFCK output when PSSL = "L".
69	DA08	O	DA08 output when PSSL = "H", WFCK output when PSSL = "L".
70	DA09	O	DA09 output when PSSL = "H", $\overline{\text{PLCK}}$ output when PSSL = "L".
71	DA10	O	DA10 output when PSSL = "H", UGFS output when PSSL = "L".
72	DA11	O	DA11 output when PSSL = "H", GTOP output when PSSL = "L".
73	VDD	—	Power supply (+5 V).
74	DA12	O	DA12 output when PSSL = "H", RAOV output when PSSL = "L".
75	DA13	O	DA13 output when PSSL = "H", C4LR output when PSSL = "L".
76	DA14	O	DA14 output when PSSL = "H", $\overline{\text{C210}}$ output when PSSL = "L".
77	DA15	O	DA15 output when PSSL = "H", C210 output when PSSL = "L".
78	DA16	O	DA16 (parallel audio data MSB) output when PSSL = "H", DATA output when PSSL = "L".
79	WDCK	O	Strobe signal output. 176.4 kHz when DF is ON, 88.2 kHz with CXD1125Q or when DF is OFF.
80	LRCK	O	Strobe signal output. 88.2 kHz when DF is ON, 44.1 kHz with CXD1125Q or when DF is OFF.

Table 7-2

Notes:

C1F1 :
C1F2 : Error correction status monitor output for C1 decode.

C2F1 :
C2F2 : Error correction status monitor output for C2 decode.

C2FL : Correction status output. Goes "H" when the currently corrected C2 series data cannot be corrected.

C2PO : C2 pointer signal. Synchronized to the audio data output.

RFCK : Read frame clock output. 7.35 MHz when locked to the crystal line.

WFCK: Write frame clock output. 7.35 MHz when locked to the crystal line.

$\overline{\text{PLCK}}$: VCO/2 output. f = 4.3218 MHz when locked to the EFM signal.

UGFS : Non-protected frame sync pattern output.

GTOP : Frame sync protect status display output.

RAOV : ±4 frame jitter absorption RAM overflow and underflow display output.

C4LR : Strobe signal. 352.8 kHz when DF is ON, 176.4 kHz with CXD1125Q or when DF is OFF.

$\overline{\text{C210}}$: C210 invert output.

C210 : Bit clock output. 4.2336 MHz when DF is ON, 2.1168 MHz with CXD1125Q or when DF is OFF.

DATA : Audio signal serial data output.

CIRCUIT DESCRIPTION

7–3. Explanation of functions

• CPU interface

1) Data input

Each register may be set by input of 4-bit address, and 4-bit data from LSB in the timing that is shown in Fig. 7–2 at three pins, XLT, CLK and DATA. The address and data of each pin are as shown in Table 7–3, and their functions are as follows. The contents of each register become entirely 0 when XRST = "L".

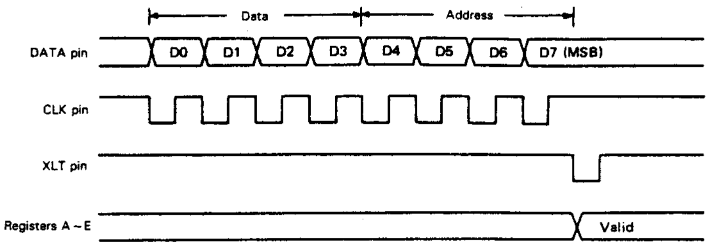


Fig. 7–2 Timing chart for data input

2) Registers

Register 9 — New function control

Controls the new functions address to the CX23035.

D0 : CRCQ — Switches ON/OFF the function which outputs the CRCF data to the SUBQ pin from the rising edge of SCOR to the trailing edge of SQCK. Details are described in "**1-(5). Subcode output**". (Page 43)

D1 : NCLV — Switches between the old CLV-P servo and the new CLV-P servo by comparison with newly added base counter. Details are described in "**6. CLV servo control**". (Page 49)

D2 : HZPD — One of the defect countermeasures. Switches ON/OFF the function which makes the PDO pin a high impedance (Z) for a maximum of 0.55 ms from the trailing edge of GFS. Details are described in "**11. Countermeasures to defects**". (Page 56)

D3 : ZCMT — Switches the zero cross mute function ON/OFF. Details are described in "**7. Interpolation and mute, attenuate**". (Page 54)

Register A — Sync. protection, attenuator control

D0 : ATTM — Used for attenuating audio signals by 12 dB.

D1 : WSEL, D2 : GSEL, D3 : GSEM — Provided for switching frame sync. protection characteristics in correspondence to the time of playback and time of access. Details will be described in the paragraph of "**2. EFM demodulation**". (Page 45)

Registers B and C — Counter set, more significant 4-bit (register C) and less significant 4-bit (register B)

These registers are used for setting the tracking counter value. The data of registers B and C are preset in the counter through the 4-bit buffer register assigned by address. Accordingly, when data of either register B or C is input, the contents of both registers are preset in the counter simultaneously as 8-bit data (either buffer register is of "OLD" data).

Register D-CLV control

D0 : GAIN — Used for setting the gain of MDP pin output in the CLV-S and CLV-H modes. It is −12 dB (time of 3/4 out of the period of RFCK/2 is of high impedance) when D0 = 0 or is 0 dB when D0 = 1.

D1 : T_P — Used for setting the period of peak hold in the CLV-S mode. Peak hold is made in the period of RFCK/4 when D1 = 0 or in the period of RFCK/2 when D1 = 1.

D2 : T_B — Used for determining the period of bottom hold in the CLV-S and CLV-H modes. Bottom hold is made in the period of RFCK/32 when D2 = 0 or in the period of RFCK/16 when D2 = 1.

D3 : DIV — Used for setting the frequency dividing ratio of RFCK, WFCK in the CLV-P mode. When D3 = 0, phase comparison of RFCK/4 and WFCK/4 is made, and output is made out of MDP pin in each case.

CIRCUIT DESCRIPTION

Register E — CLV mode

It is as shown in Table 7–3.

The details of each mode will be described in "**6. CLV servo control**". (Page 49)

D3 to D0 are all "0" when XRST = L.

Register name	Command	Address D7 ~ D4	Data D3	D2	D1	D0	SENS pin
.9*1	New function control	1001	ZCMT	HZPD	NCLV	CRCO	Z
A*2	Sync protection attenuator control	1010	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set, Less significant 4-bit	1011	Tc3	Tc2	Tc1	Tc0	$\overline{\text{COMPLETE}}$
C	Counter set, More significant 4-bit	1100	Tc7	Tc6	Tc5	Tc4	$\overline{\text{COUNT}}$
D*3	CLV control	1101	DIV	T_B	T_P	GAIN	Z
E*4	CLV mode	1110	CLV mode				$\overline{\text{PW} \geqq 64}$

***1 Register 9**

		Dn = 0	Dn = 1
ZCMT	D3	Zero-cross MUTE off	Zero-cross MUTE on
HZPD	D2	PDO pin is always active.	PDO pin is "Z" at the trailing edge of GFS.
NCLV	D1	CLV-P servo for the frame sync signal	CLV-P servo for the base counter
CRCQ	D0	CRCF is not superimposed on SUBQ	SUBQ = CRCF at the raising edge of SCOR

***2 Register A**

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTG pin	dB
0	0	0
0	1	−∞
1	0	−12
1	1	−12

***3 Register D**

DIV	D3	0	RFCK/4, WFCK/4	Phase comparison frequency in CLV-P mode
		1	RFCK/8, WFCK/8	
T_B	D2	0	RFCK/32	Bottom hold period in CLV-S, CLV-H mode
		1	RFCK/16	
T_P	D1	0	RFCK/4	Peak hold frequency in CLV-S mode
		1	RFCK/2	
GAIN	D0	0	−12 dB	Gain at MDP pin in CLV-S, CLV-H mode
		1	0 dB	

***4 Register E**

Mode	D3 ~ D0	MDP pin	MDS pin	FSW pin	MON pin
STOP	0000	L	Z	L	L
KICK	1000	H	Z	L	H
BRAKE	1010	L	Z	L	H
CLV-S	1110	CLV-S	Z	L	H
CLV-H	1100	CLV-H	Z	L	H
CLV-P	1111	CLV-P	CLV-P	Z	H
CLV-A	0110	CLV-S or CLV-P	Z or CLV-P	L or Z	H

Z: High impedance

Table 7–3 List of registers

CIRCUIT DESCRIPTION

3) Tracking counter

This counter is provided for facilitating track jump. Load the number of tracks to be jumped in registers B and C. Count of CNIN pulses is started at rising edge of XLT after it was loaded in either register B or C.

When n (n = 256 is meant when register B = register C = 0) is loaded in registers and the address is set at "B", a signal $\overline{\text{COMPLETE}}$ that is of HIGH level up to "n" pulses and is of LOW level after "n" pulses is output of SENS pin. When the address is set at "C", signal $\overline{\text{COUNT}}$ of CNIN/2n (Hz) is output.

The tracking counter timing chart ia shown in Fig. 7–3.

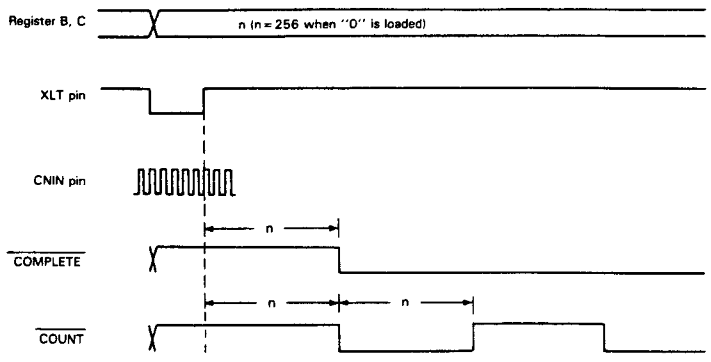


Fig. 7–3 Tracking counter timing chart

4) SENS

The following signals are output from SENS pin depending on the address of D7 ~ D4.

(1) $\overline{\text{COMPLETE}}$: Address (see note) is "B"; Shown in Fig. 9.

(2) $\overline{\text{COUNT}}$: Address (see note) is "C"; Shown in Fig. 9.

(3) $\overline{\text{PW≧64}}$: Address (see note) is "E"; This signal is of LOW level when the pulse width after bottom hold is over 63, and is of HIGH level otherwise. It is used for detection of a drop in the speed of the spindle motor after braking and so on.

Note: Address setting is determined by the data corresponding to D4 to D7, which are input from the DATA pins shown in Fig. 7–2.

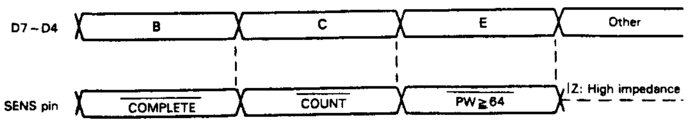


Fig. 7–4 Timing chart of SENS pin

DP-720

CIRCUIT DESCRIPTION

5) Sub code output

Sub codes P ~ W loaded in the 8-bit shift register are output out of SBSO pin in accordance with the clock input through EXCK pin. When SCOR pin is "H", S0 + S1 signal is output. Sub code Q is as follows, depending on the SQEX pin status.

a. When the SQEX pin is "L", sub code Q is output from the SUBQ pin in synchronism with the WFCK signal in the same way as for the CX23035. The $\overline{\text{WFCK}}$ is also output from the SQCK pin.

b. When the SQEX pin is "H", sub code Q is output from the SUBQ pin in synchronism with the external clock (as from the microprocessor). Two 80-bit shift registers, for reading and writing, are incorporated as shown in Fig. 7–8 and while the microprocessor reads, the new sub code Q is written to another register. The microprocessor is interrupted from the outside at the rising edge of the SCOR pin, and after checking the CRCF flag (output to the CRCF pin, or the SUBQ pin when the CRCQ flag is "1"), the CRCF is checked. If CRCF = "H", a shift lock is output and the new sub code Q is read. After the LSB side is replaced with the MSB side by a unit of 4-bit, the data is stored in register. As the microprocessor serially inputs from the LSB first, replacing the 4-bit of data is unnecessary.

(a) Timing of SBSO, SUBQ, SCOR, CRCF

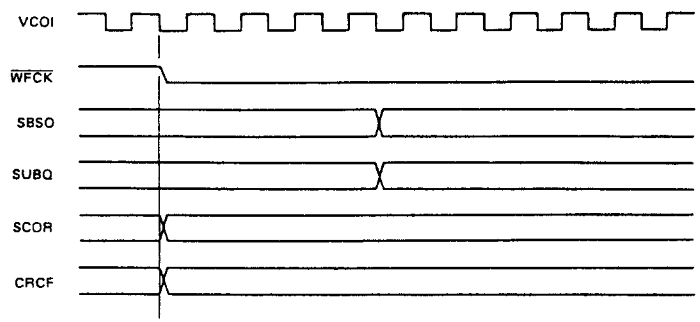
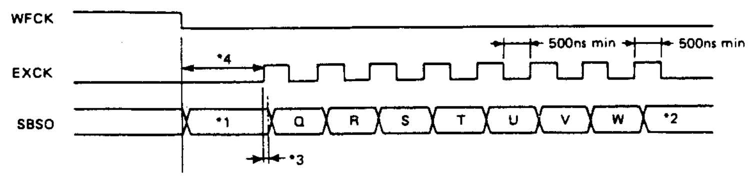


Fig. 7–5

(b) Timing of SBSO, EXCK



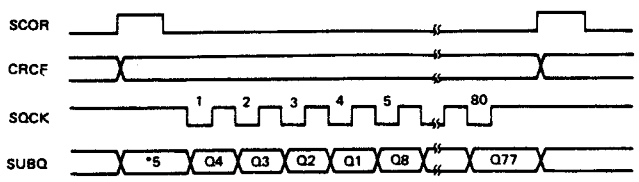
*1: Sub code P is output when SCOR is 0.
S0 + S1 is output when SCOR is 1.
*2: SBSO is 0 when 8 or more pulses are input to EXCK.
*3: 4T ~ 6T if the period of VCO is expressed as T.
*4: Make EXCK low for 10 μs from the rising edge of WFCK.
One time period of T = 8.6436 MHz.

Fig. 7–6 Timing chart of sub code outputs

CIRCUIT DESCRIPTION

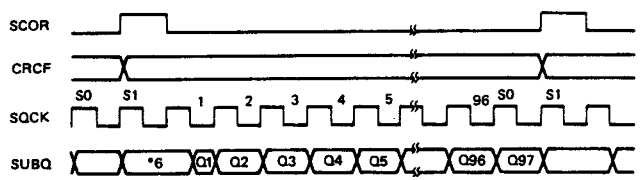
(c) Timing of SCOR, CRCF, SQCK, SUBQ

SQEX = "H" level



*5: CRCF when CRCQ flag is "1", undefined when "0".

SQEX = "L" level



*6: CRCF when CRCQ flag is "1", Q98, Q1 when "0".

Fig. 7–7 Timing chart of sub code outputs

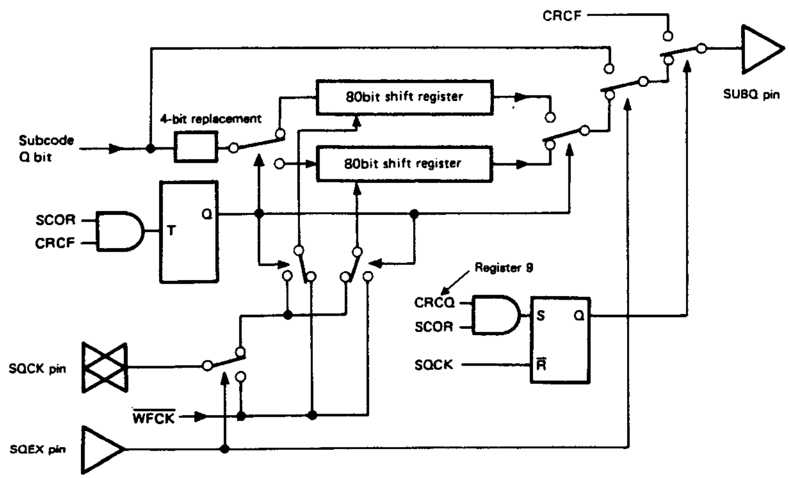


Fig. 7–8

DP-720

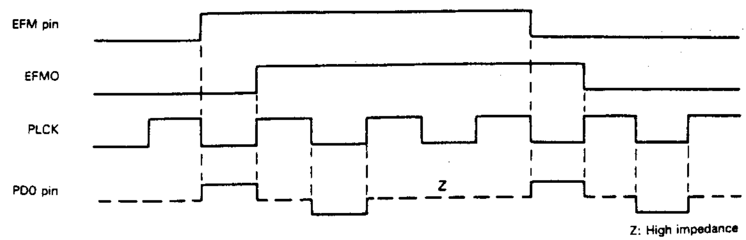
CIRCUIT DESCRIPTION

- **EFM demodulation**

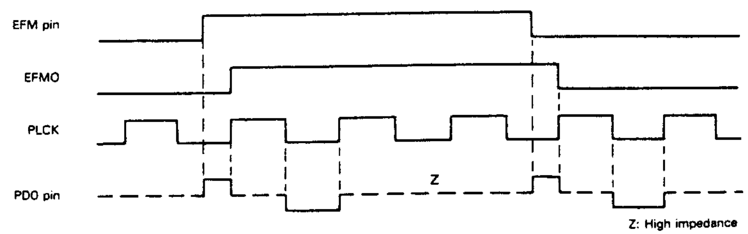
1) Playback of bit clock by EFM-PLL circuit

The EFM signal read out of the optical block contains a clock component of 2.16 MHz. Therefore, it is possible to take out a bit clock (PLCK) of 4.32 MHz synchronized with this clock by the EFM-PLL circuit.
At each edge of EFM signal, phase comparison is made with PLCK, which is 1/2 of VCO, is made and output is made by TRI STATE out of PDO pin. The mean value of PDO pin is about 1/2 VDD if synchronized, but the mean value drops when VCO becomes higher. On the other hand, the mean value increases when VCO becomes less.
The timing charts of EFM pin, EFMO, PLCK and PDO are shown in Fig. 7–9.

(a) When EFM signal and VCO are synchronized



(b) When VCO is higher than EFM signal



(c) When VCO is less than EFM signal

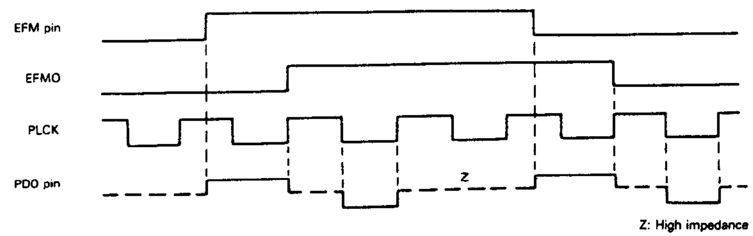


Fig. 7–9 Timing chart of EFM-PLL circuit

CIRCUIT DESCRIPTION

2) Detection, protection and interpolation of frame synchronizing signals

There are cases during recording where the same pattern is detected in the data due to the influence of drop-out and jitter, even if a pattern that is same as the synchronizing signal will not appear.
On the other hand, there also are cases where original frame synchronizing signal is not detected. Therefore, protection and interpolation are required besides detection.
The edge portion only of EFM signal (EFMO) latched with PLCK is converted to "1" and the rest to "0", and then input is to a 23-bit shift register and a frame synchronizing signal is detected.
In order to protect a frame synchronizing signal, a window is provided and the same patterns outside of this window are removed. This width can be selected with WSEL.
If no frame synchronizing signal is located in this window, interpolation is made with a signal produced by 588-mal counter (4.3218 MHz/588 = 7.35 kHz)
A 4-bit counter for counting the number of these frames to be interpolated is provided, and when its count reaches the level selected with GSEL, GSEM, the window is ignored and the 4-bit counter is reset with the next frame synchronizing signal. The GTOP pin is of "H" while this operation is performed. Further, GSF pin is of "H" when the frame synchronizing signal generated by the 588-mal counter for making interpolation is synchronized with the frame synchronizing signal from the disc.
The frame synchronizing signal before passage through the window or the window is output out of UGFS (DA05 pin at the time when PSSL = L).

WSEL	Window width
0	±3 clock
1	±7 clock

GSEM	GSEL	Number of frame to be interpolated	UGFS (PSSL = L)
0	0	2 frames	Window
0	1	4 frames	Window
1	0	8 frames	Frame synchronizing signal before passage through window.
1	1	13 frames	Window

The timing for write request signal (WREQ). Write Frame Clock (WFCK), etc. is generated based on the protected and interpolated frame synchronizing signal.

3) EFM demodulation

14-bit data is taken out of the 23-bit shift register and is demodulated to 8-bit data through 14 → 8 conversion circuit composed of array logics. Then a write request (WREQ) signal is output to the RAM interface block, and the data is then output to the data bus (DB08 - DB01 pins) of the RAM in accordance with the OENB signal transmitted from said block.

● Sub code demodulation

1) Sub code demodulation

Synchronizing signals S0 and S1 of 14-bit sub codes are detected out of the 23-bit shift register, and sampling is made in the timing that is synchronized with WFCK.
After delay of S0 by one frame, S0 + S1 is output out of SCOR pin and S0 · S1 is output out of SBSO pin (only when SCOR = H).
Data (P - W) of sub codes only is input to the register in the timing synchronized with WFCK after EFM demodulation; and sub code Q is output out of SUBQ pin, and at the same time, it is loaded in the 8-bit shift register and is output out of SBSO pin in correspondence to a clock from EXCK pin.
The details of this timing will be shown in **"1. CPU interface"**. (Page 40)

2) Sub code Q error detection

The CRC result of sub code Q is output from the CRCF pin in synchronism with the SCOR pin.
It goes "L" when an error is detected. If the CRCQ flag is "1" at this time, the CRCF flag is output from the SUBQ pin during the time from the rising edge of the SCOR pin to the trailing edge of the SUBQ pin. This timing is detailed in **"1. CPU interface"**.

CIRCUIT DESCRIPTION

● RAM interface (generation of external RAM address)

1) Request from EFM demodulation block (Write RAM request)

When one symbol of demodulation is complete in the EFM demodulation block requests to write data to the external RAM to the RAM interface block. This request is WREQ signal.
This block gives priority orders to requests from other blocks and processes these requests.
When EFM write request is received, an address is generated to the RAM and Write Enable state is produced. Furthermore, a data output instruction is issued against the EFM demodulation block. This instruction is OENB signal.
Clocks of PLL system are used for EFM block and for requests (WREQ) from EFM block, but clocks of X'tal system are used for processing thereafter.

2) Request from D/A converter output circuit (Read to D/A request)

This is a de-interleaved data request issued out of the timing generator in this block.
This request is of the highest priority among all requests, and addresses of three types are generated against this request.
This request is generated once every 24 periods based on the period of system clock **C212 (8.4672 MHz/4)**. The data output out of the RAM is C2 pointer first, less significant 8-bit out of 16-bit and finally more significant 8-bit.

3) Request from error correction block (C1/C2 correction, pointer R/W)

The error correction block requests the data located on the system (C1/C2) to be corrected. Furthermore, there is a request to rewrite incorrect data to correct data.
In addition, there is a request for pointer R/W which indicates reliability of data.
These requests are made by the 8-bit data directed to the RAM interface block from the error correction block.
The requests from the error correction unit are of the lowest priority among requests of three types.
After acceptance of a request, data from RAM is directed to the 3rd clock of C212.
The data of acceptance of a request is output to the error correction block as a PREN signal.
This block generates type address of the requested data, and controls R/W of the RAM at the same time.

4) Address generation

The data after EFM demodulation is data subjected to interleave processing.
This interleave processing is subjected to data lag by the unit of a frame.
Data of 108 frames are required for de-interleave. In other words, for obtaining one frame of audio data played in a certain length of time, data of 108 frames after EFM demodulation are required. Further, the system data of C1/C2 is of the system in the process of application of interleave, and therefore, is included in 108 frames.
Data in practice are generated continuously. That is, de-interleave should be updated by the unit of a frame.
Therefore, Read/Write base counters are required. This base counter performs counting by the unit of a frame.
The writer base counter is used only at the time of EFM data writer.
The address directed to the external RAM is determined by the relative lag value to EFM demodulation data and their number of frames.

5) Priority of address generation request

The system control block determines priority of address generation requests made to the RAM interface block.
The priority order is as follows, beginning with higher priority.

1. Read to D/A request
2. Write to RAM request
3. C1/C2 request

The number of times of requests is as follows.

1. Requests of 12 times in the frame section
   The number of times of address generation to it is 36 times.
2. Requests of 32 times in the frame section
   The number of times of address generation to it is 32 times.
3. Maximum number of times of request (C1 Double error correction, C2 pointer copy)
   Read R/W 64 times, Point R/W 65 times in one frame section
   The number of times of address generation to it is 129 times.

CIRCUIT DESCRIPTION

288 C212 (clocks) are included in a frame, and the number of times of operation of the RAM in it is 197 times at maximum.
In the system control block, against request 1, the timing of its occurrence is reserved in advance. Requests 2, 3 are generated simultaneously, priority is given to request 2, and if a request is generated during execution of either request, priority is given to the job in execution.

6) Jitter margin

The EFM demodulation data is synchronized with data's playback system (PLL) as described earlier. Accordingly, it includes disturbance (wow, flutter, etc.) of disc rotation servo, etc. It is loaded to the external RAM. As the data taken out of the RAM is synchronized with the clock of X'tal system, this RAM is subjected to time axis correction.
However, the limit of time axis correction is determined by the capacity of the RAM. In this system, other data is destroyed when read/write frames are spaced apart by ±5 frames. In such a status how the playback sound is cannot be guaranteed. The base counter monitor is provided in order to avoid it.
In other words, when the difference between read base counter and write base counter exceeds ±4 frames, the write base counter is set in the value of the read base counter.
As a result, there is no case where data without error correction is output to the D/A.
The RAOV signal is of ''H'' for one frame (WFCK) section when the difference between base counters exceeded ±4 frames.

• Error correction

(1) The error correction block makes correction up to double errors with each of C1 correction and C2 correction.
(2) This system adopts a unique pointer erasure method in order to minimize erroneous correction. Accordingly, the external 16K RAM stores these pointer data in addition to audio data.
(3) The pointer generated in C1 correction is called C1 pointer and the pointer generated in C2 correction is called C2 pointer.
(4) When the data of C1 system is judged as reliable, a C1 pointer is set in this system.
(5) During C2 correction, whether correction is to be made or not to be made and whether the data is reliable or unreliable are judged from the error location, locations and number of C1 pointers obtained through computation. A C2 pointer is set against an unreliable word (16-bit).
(6) The word in which a C2 pointer was set is subjected to previous value hold or mean value interpolation when it is output out of this LSI.
(7) Terminal C2FL becomes ''H'' when one or more C1 pointers are set in the data included in the C2 system at the time of C2 correction. C2FL is reset to ''L'' in minimum 472ns (see Note) after deactivation of pin RFCK. C2FL is the AND of C2F1 and C2F2.

Note: 472ns: One period of 2.1168 MHz

(8) The flow of data with the external RAM is as follows.

A data request is made from the correction block to the RAM interface block.

↓

The RAM interface block accepts the request with the operating situation of the entire system observed. The address of the requested data is generated to the external RAM.

↓

Read/Write of the correction block and RAM data are enabled.

(9) When PSSL is set at ''L'', a signal that is capable of monitoring error correction is output.
C1F1, C1F2, C2F1 and C2F2 output to DA01 - DA04 are these monitor signals. These signals are reset to ''L'' when a period of minimum 472ns has elapsed since deactivation of RFCK.
The levels and meanings of these signals at the time of deactivation of RFCK are as follows.

CIRCUIT DESCRIPTION

C1F1	C1F2	C1 correction status
0	0	No error
1	0	Single error correction
0	1	Double error correction
1	1	Irretrievable error

C2F1	C2F2	C2FL	C2 correction status
0	0	0	No error
1	0	0	Single error correction
0	1	0	Double error correction
1	1	1	Irretrievable error

• CLV servo control

The spindle motor revolution is controlled with one selected out of the following seven modes in accordance with a command from the CPU. CLV is the abbreviation of Constant Linear Velocity. The output is composed of MDP pin for controlling synchronization of velocity and phase, MDS pin for controlling synchronization of velocity, FSW pin for making selection of filter constant and MON pin for controlling motor ON/OFF.

(1) **STOP:** Register E = 0000'B (B means binary)
Mode for stopping the spindle motor.
MDP = FSW = MON = ''L'', MDS = ''Z''

(2) **KICK:** Register E = 1000'B
Mode for running the spindle motor in forward direction.
MDP = MON = ''H'', MDS = ''Z'', FSW = ''L''.

(3) **BRAKE:** Register E = 1010'B
Mode for running the spindle motor in reverse direction.
MDP = FSW = ''L'', MDS = ''Z'', MON = ''H''.

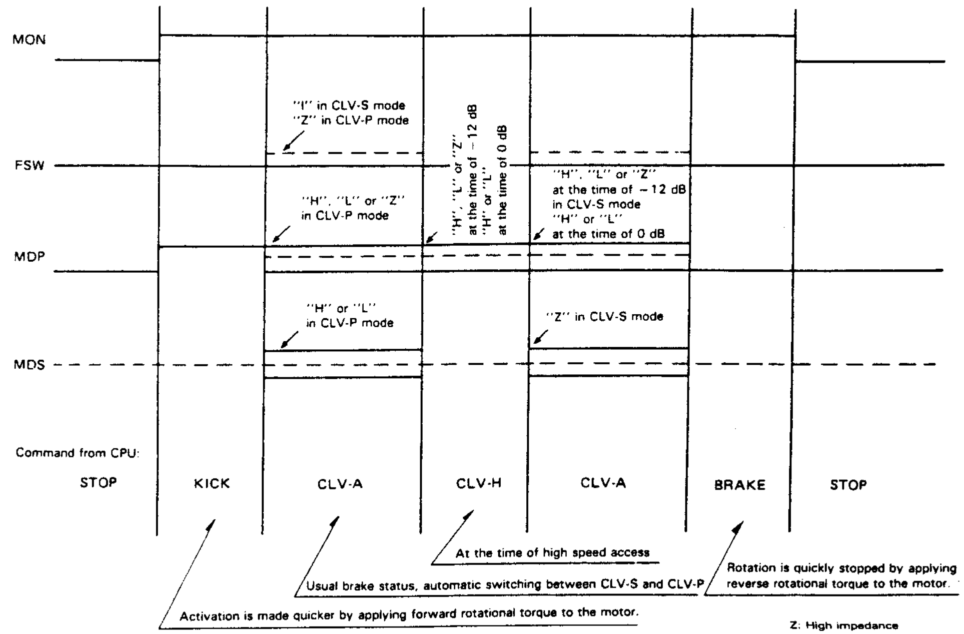


Fig. 7–10 Typical control of spindle motor

CIRCUIT DESCRIPTION

(4) CLV-S: Register E = 1110'B
Rough servo mode used at the time of start of rotation, at the time of track jump and also when the EFM-PLL circuit is unlocked due to another reason.
When the period of VCO's oscillation frequency 8.6436 MHz is expressed as "T", the pulse width of a frame synchronizing signal is "22T" during specified revolution, and it is the maximum pulse width in a period of RFCK. In practice, however, there are pulses having widths over "22T" due to drop-off of EFM signal due to other reasons, and the frame synchronizing signal cannot be correctly detected unless such pulse are removed. Therefore, the maximum value (peak) of the pulse width of EFM signal is detected (called peak hold) in the period of RFCK/2 or RFCK/4, than the minimum value in this peak is detected (called bottom hold) in the period of RFCK/16 or RFCK/32, and this value is used as the frame synchronizing signal.
"L" is produced out of MDP pin while the frame synchronizing signal is "21T" or less, "Z" when it is "22T", or "H" when it is "23T" or more. Either 0 dB or 12 dB can be selected as its gain.
MDS = "Z", FSW = "L", MON = "H".

(5) CLV-H: Register E = 1100'B
Rough servo mode used at the time of high-speed access.
Assuming there are 20,000 tracks, from the innermost to the outermost, and that this distance is accessed in 1 second, the mirrors (portions where there are no pits) between tracks result in a 20 kHz signal, which is superimposed on the EFM signal. When such a signal is input in the CLV-S mode, a longer mirror section than the actual frame sync signal is detected as the peak value, resulting in an unstable servo.
Therefore, in order to stabilize the servo during high-speed access, the CLV-H mode performs the peak hold at a period of 8.4672/256 MHz (about 34 kHz). Then, like the CLV-S mode, it performs the bottom hold at a period of RFCK/16 or RFCK/32. Except for the period of peak detection, other operations of the CLV-H mode are the same as for the CLV-S mode.

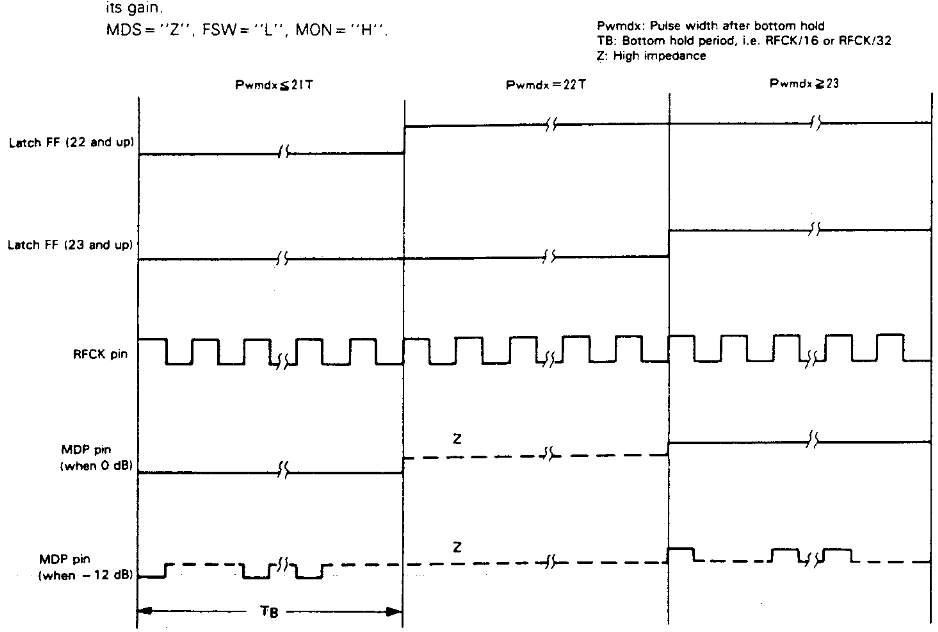


Fig. 7—11 Timing chart in CLV-S, CLV-H mode (1)

CIRCUIT DESCRIPTION

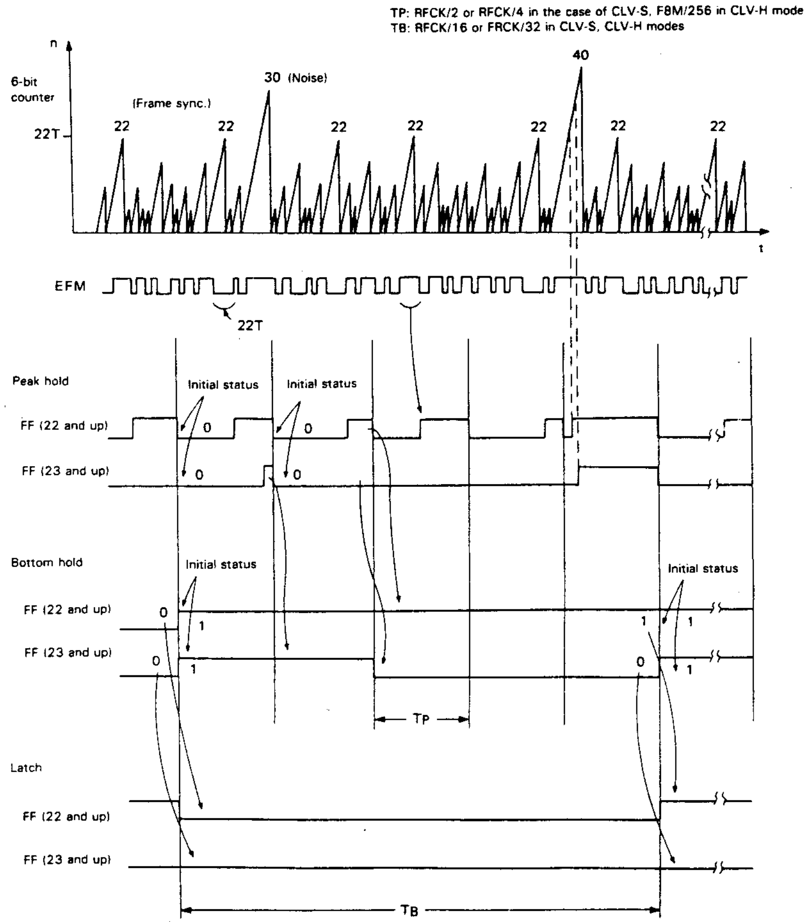


Fig. 7—12 Timing chart in CLV-S, CLV-H mode (2)

CIRCUIT DESCRIPTION

(6) CLV-P: Register E = 1111'B

PLL servo mode.

When the NCLV of register 9 is "0", the phase of the WFCK/4 signal and the phase of the RFCK/4 signal are compared and output to the MDP pin. When NCLV = "1", 1/4 of the base counter frame frequencies at the Write side and the Read side are phase-compared and output to the MDP pin. It goes "H" when WFCK is slow, "L" when it is fast, and is "Z" when synchronized.

Assuming the 8.4672/2 MHz period is T, and the time when WFCK is "H" is thw, the MDS pin outputs a signal which goes "H" during the time from the trailing edge of WFCK to the time represented by $(thw-279T) \times 32$, and then goes "L" until the next trailing edge of WFCK.

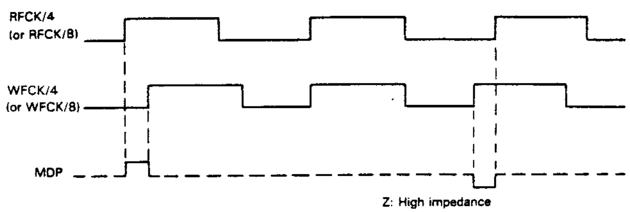
MDS = "H" when thw $\geqq$ 279T,

MDS = "L" when thw $\leqq$ 279T.

The MDS pin varies between 32T and 544T, in 32T steps, when 280T $\leqq$ thw $\leqq$ 296T. For example, when synchronized (rotating at the standard speed), that is when thw = 288T, a 7.35 kHz signal, with a duty cycle of 50% is output.

FSW = "Z", MON = "H"

MDP pin



MDS pin (The period of 4.2336 MHz is expressed as "T".)

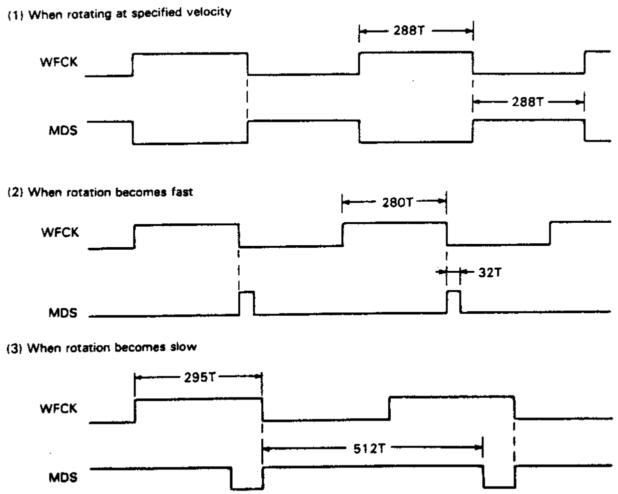


Fig. 7–13 Timing chart in CLV-P mode

CIRCUIT DESCRIPTION

(7) CLV-A: Register E = 0110'B

The mode used for normal play status.

The GFS signal ("H" when locked, "L" when unlocked), after frame sync detection, protection and interpolation block, is sampled at WFCK/16, and functions in CLV-P mode when the signal is "H". When the "L" signal continues for 8 times, the mode is automatically changed to CLV-S mode.

When in the CLV-S mode, setting of the peak hold period, and setting of the period and gain of the bottom hold of the CLV-S and CLV-H are performed in register D, and the selection of each mode is performed in register E. The description of these registers are detailed in **"1. CPU interface".** (Page 40)

Note:

When PSSL = "L", DA07 pin outputs WFCK/4 or WFCK/8 as FCKV, and DA08 outputs EFCK/4 or EFCK/8 as FCKX.

(8) CLV-A': Register E = 0101'B

New auto servo mode added to the CX23035.

The difference between CLV-A' and CLV-A is in the rough servo system. With the old rough servo system, the EFM pattern is measured by a crystal and the servo is applied so that the width of the sync pattern is a fixed value, and the rotation speed of the spindle motor is roughly fixed. In this case, if the value is out of the VCO capture range, the VCO never locks with the EFM. With the new rough servo system, a VCO is used for measurement instead of a crystal. If the VCO center is shifted from true center the VCO tends to lock, since the rotation of the spindle motor varies in the same direction.

The new rough servo functions only in CLV-A' mode. The rough servo in CLV-A mode and CLV-S mode is the old rough servo.

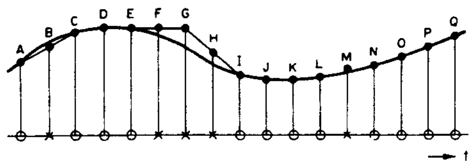
CIRCUIT DESCRIPTION

• Interpolation and mute, attenuate

1) Interpolation circuit block

3-byte data can be obtained with a Read to D/A request. They are C2 pointer, less significant 8-bit and motor significant 8-bit. The total 16-bit constitute the data generated per sampling (2's complement.)

The C2 pointer expresses the reliability of this 16-bit data. Therefore, data with C2 pointer is subject to interpolation in this block.



O: Without C2 pointer
X : With C2 pointer

Fig. 7–14

Mean value interpolation

$B=\frac{1}{2}(A+C)$

$H=\frac{1}{2}(E+I)$:.When pointers are continuous

$M=\frac{1}{2}(L+N)$

Previous value hold

F = G = E

16-bit data is alternately output to L-ch and R-ch, R-ch data is output in the section in which LRCK is "L" and L-ch data is output in the section in which LRCK is "H".

C2PO signal outputs C2 pointer to the 16-bit data directed DA01 - DA16 (PSSL = H), DA16 (PSSL = L).

In other words, it means that the 16-bit data that is output when C2PO is "H", is interpolated data.

2) Explanation of muting and attenuator

In the muting block it is possible to mute ($-\infty$ dB) or attenuate (-12 dB) the audio signal in accordance with the MUTG pin and ATTM signal of the CPU interface block.

When the ZCMT flag of register 9 is "1", the input from the MUTG pin is valid only if all of the audio data higher 6-bit (including the sign bit) are "1" or "0".

Note that switching the MUTG pin does not cause muting if the data zero-cross does not occur. To eliminate this problem, after switching the MUTG pin "H" or "L" with ZCMT = "1", ZCMT shall be turned "0" in a specified period of time, regardless of whether the zero-cross causes muting ON/OFF or not.

ATTM	MUTG	Attenuation value	Remarks
0	0	0 dB	
1	0	-12 dB	
0	1	$-\infty$ dB	(See Note)
1	1	-12 dB	(See Note)

Note:
When the MUTG is set to "H" level with the NCLV flag set to "0", the read base counter value is continuously loaded into the write base counter as well as the muting.
Except at CLV-A, CLV-P, CLV-S, or CLV-A' with the NCLV flag set to "1", the base counter value is loaded.

CIRCUIT DESCRIPTION

• Mode setting

The various kinds of mode can be set by combining the following pins. (Refer to Table 7–4.)

MD1 pin : Mainly for selection of the oscillator clock at the XTAI or XTAO pin.
MD2 pin : Mainly for selection of the digital out function.
MD3 pin : Mainly for selection of the digital filter function.
PSSL pin : Mainly for selection between serial and parallel output.
SLOB pin : Selection between offset binary and 2's complement.

Input pin					Function					(Note)	Compatible IC	
MD1	MD2	MD3	PSSL	SLOB	8M/16M	DO OFF/ON	DF OFF/ON	P/S	OB/2's	CD ROM/AUDIO	CXD1125	CXD1130
L	L	L	L	L	16M	DO ON	DF ON	Seri	2's	AUDIO		
L	L	L	H	H	↓	↓	↓	Para	OB	↓		
L	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	
L	H	L	L	L	↓	DO OFF	DF ON	↓	↓	↓		○
L	H	L	H	H	↓	↓	↓	Para	OB	↓		○
L	H	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
L	H	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	L	L	L	L	8M	↓	DF ON	Seri	2's	↓		○
H	L	L	H	H	↓	↓	↓	Para	OB	↓		○
H	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
H	L	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	H	H	L	L	16M	DO ON	↓	Seri	2's	CD ROM	○	
H	H	H	H	L	8M	DO OFF	↓	↓	↓	↓	○	○

Note:
• 8M/16M: Selection of clock, XTAI or XTAO. 8.4672 MHz/ 16.9344 MHz
• DO OFF/ON: Digital out OFF/ON
• DF OFF/ON: Digital filter OFF/ON
• P/S: Parallel output/serial output
• OB/2's: Offset binary/2's complement
• CD ROM/AUDIO: Compatible to CD ROM/Compatible to audio

Table 7–4

• Selection of clock

The oscillator clock for XTAI and XTAO is available at 16.9344 MHz and 8.4672 MHz. However, when digital output is used, the clock must be set to 16.9344 MHz.

• Selection of digital filter (Refer to "9. Digital filter".)

When the digital filter function is set to ON, the DAC interface signal are all set to double speed.

• Selection of parallel output/serial output

When the parallel output is selected, DA01 to DA16 pins output the 16-bit parallel data.

When the serial output is selected, DA01 to DA16 pin output the following signals respectively.

C1F1 (DA01) : Error correction status monitor output at
C1F2 (DA02) : C1 decode.
C2F1 (DA03) : Error correction status monitor output at
C2F2 (DA04) : C2 decode.
C2FL (DA05) : Correction status output, C2FL = C2F1·C2F2.
C2PO (DA06) : C2 pointer signal.
RFCK (DA07) : Read frame clock signal, 7.35 kHz when locked to the crystal line.
WFCK (DA08) : Write frame clock signal, 7.35 kHz when locked.
$\overline{\text{PLCK}}$ (DA09) : 1/2 of the divided signal from the VCO pin, 4.3218 MHz when locked.
UGFS (DA10) : Non-protected frame sync signal.
GTOP (DA11) : Frame sync protect status display signal.
RAOV (DA12) : Jitter margin over or underflow display signal.
C4LR (DA13) : 4 times the LRCK signal.
$\overline{\text{C210}}$ (DA14) : Bit clock (invert signal of $\overline{\text{C210}}$).
C210 (DA15) : Internal system clock (4.2336 MHz when DF is ON, 2.1168 MHz when CXD1125Q or DF is OFF).
DATA (DA16) : Serial data output (MSB or LSB first output).

CIRCUIT DESCRIPTION

• Selection of offset binary/2's complement
When the SLOB pin is "H", an offset binary signal is output, and when it is "L", a 2's complement signal is output.

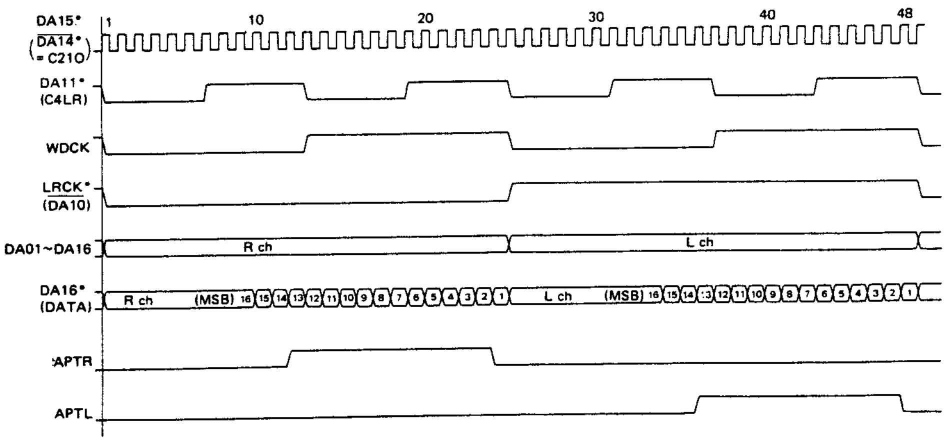
• Selection of CD ROM/audio compatibility
When MD1 = MD3 = "H", the player is compatible with a CD ROM and outputs the C2 pointer for each byte. At the same time, the average value interpolation and the previous value holding operations are not performed. For example, when there is an error in the upper 8-bit of the 16-bit, only the C2 pointer corresponding to the upper 8-bit goes "H", and the lower 8-bit are processed as the correct data.

• Digital filter
The built-in digital filter has the following features:
1. Correction of the aperture effect
2. Small attenuation at 20 kHz
3. Practical-design filtering band ranges

• Digital audio (D/A) interface
The player incorporates a D/A interface output (digital output) and the digital signal is output from the DOTX pin. The digital signal is output after passing through interpolation, mute and attenuator circuits. The 4 control bits (ID0, ID1, COPY, EMPHASIS) in the C-bit channel status perform a CRC check and are revised only when it's OK.

• Countermeasures to defect
To counter a defect, the PDO pin is set to "Hi-Z" during the time until GFS goes "H" again after inverting from "H" to "L" or after about 0.55 ms has elapsed. However, this operation is performed only when the HZPD flag of register 9 is "1". When HZPD = "0", it will never be set to "Hi-Z".
The signal switching between the rough servo in the CLV-A or CLV-A' mode and the PLL servo is output from the LOCK pin.
After the GFS signal is sampled at WFCK/16, and when the signal is "1", the LOCK pin goes "H", when a "0" is present 8 times in a row, the LOCK pin goes "L".
This operation is similar to that for the FSW pin.
However, while the FSW outputs a fixed signal when not in CLV-A or CLV-A' mode, the LOCK pin always output the above signal.

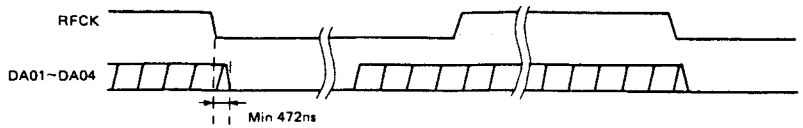
• Timing chart



* When PSSL = "L".

Fig. 7–15 Timing chart of audio output

CIRCUIT DESCRIPTION



* DA01 to DA04 (C1F1, C1F2, C2F1, C2F2) are cleared when a period of minimum 472 ns has elapsed since RFCK was deactivated.
* AND signal of C2F1 and C2F2 is output out of C2FL pin.

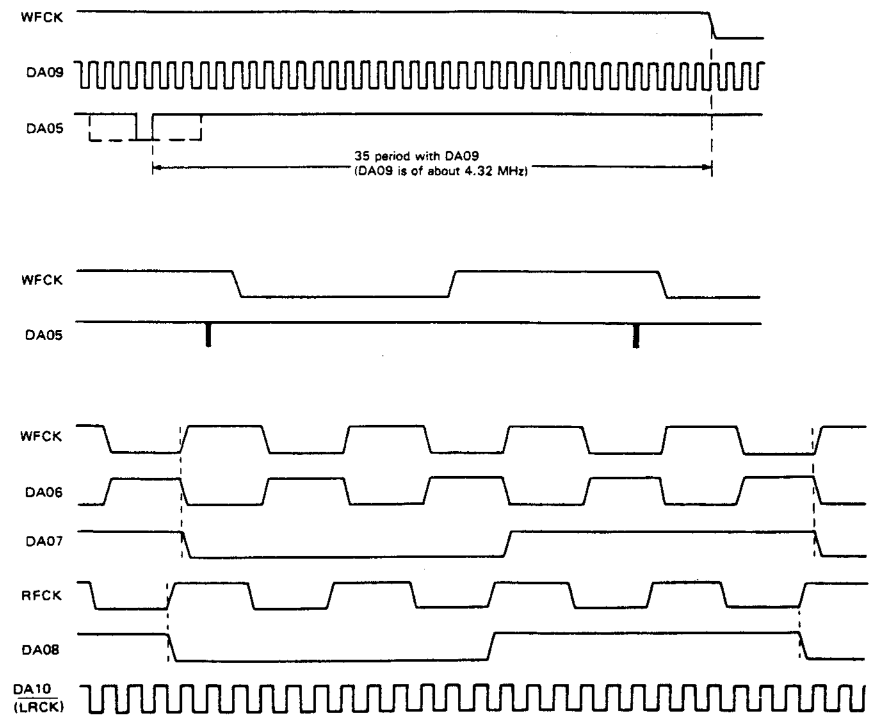


Fig. 7–16 Timing chart of DA01 to DA16 output when PSSL = "L"

CIRCUIT DESCRIPTION

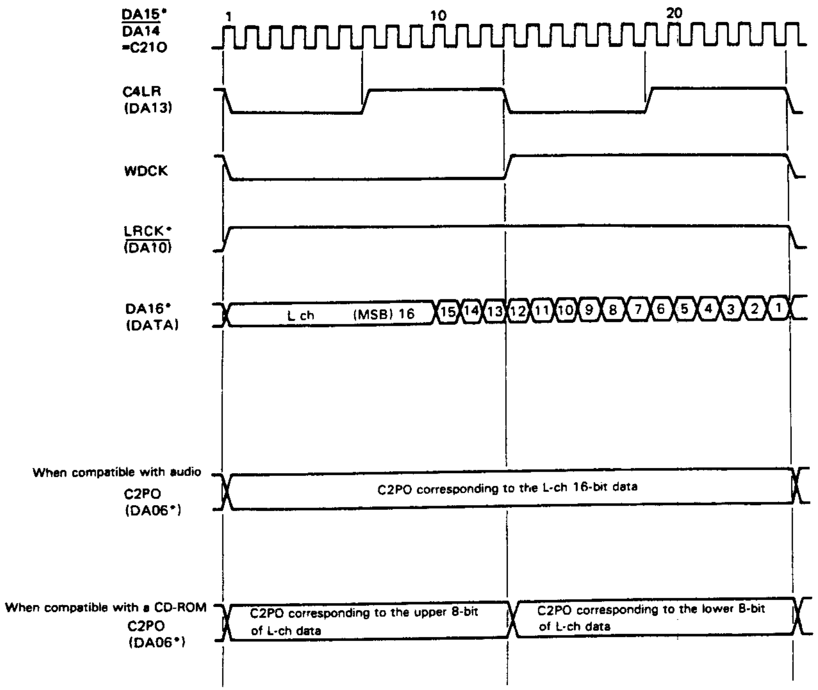


Fig. 7–17 Timing chart of C2PO output (when PSSL = "L")

* RAOV becomes "H" for one frame (synchronized with WFCK) when a jitter that exceeds ±4 frames is generated between RFCK and WFCK.

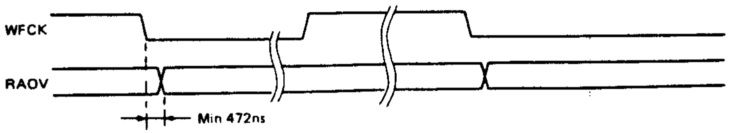


Fig. 7–18 Timing chart of RAOV output

CIRCUIT DESCRIPTION

8. D/A Converter TD6720N (X32-1260-23, X32-1262-73 : IC8) Japan made (X32-1302-72 : IC8) Singapore made

TD6720N is a 16-bit Hi-Fi D/A converter of dual slope single integration type developed for PCM digital audio devices.

- This converter can be applied to 2's compliment code.
- This converter has a sampling holding circuit in it, thus the number of parts to be installed outside can be reduced.
- Sampling frequency of 30kHz to 100kHz can be applied to this converter. (This can be used as a double over-sampling D/A converter for CD player and DAT.)
- This converter has crystal oscillator amplifier in it.
- This converter outputs clock SCK of 1/4 frequency of f crystal.
- This converter performs D/A conversion of the signals of right and left channels alternately.

8–1. Terminal connection diagram

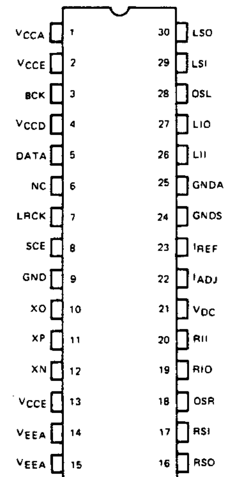


Fig. 8–1

8–2. Block diagram

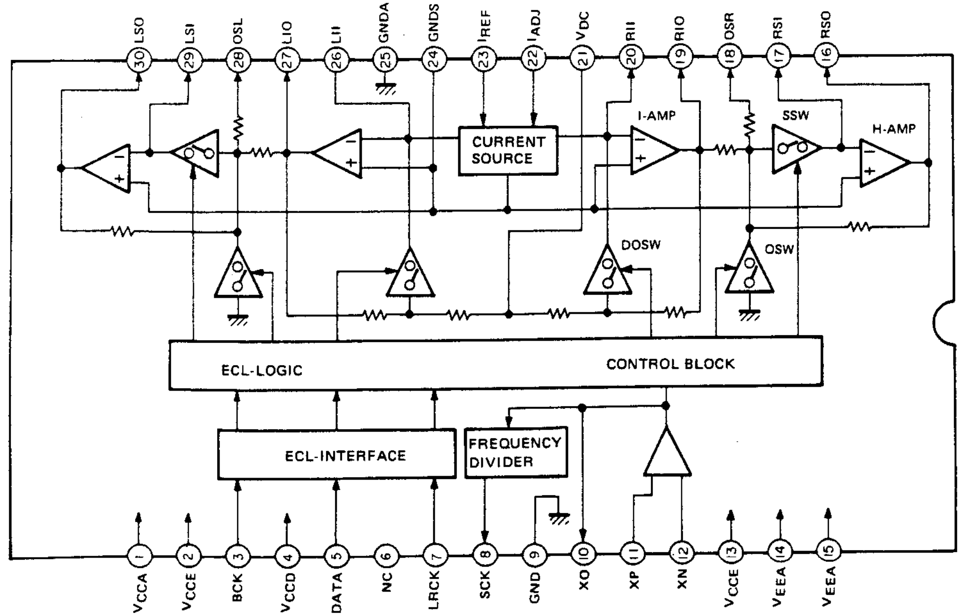


Fig. 8–2

CIRCUIT DESCRIPTION

8–3. Terminal description

Terminal No.	Terminal Name	Function
1	VCCA	Analog circuitry positive power supply voltage terminal. (+5V)
2	VCCE	ECL logic power supply voltage terminal. (+5V)
3	BCK	Bit clock input terminal. Duty cycle = 50%, f = 1.4112MHz.
4	VCCD	Digital circuitry power supply voltage terminal. (+5V)
5	DATA	PCM digital audio data input terminal. Data is input in synchronism with the negative-going edge of BCK, in bit-serial from the MSB (per 16 bits basis).
6	NC	No connection.
7	LRCK	Input data L/R ch indication signal input terminal. Signal must be input in synchronism with the negative-going edge of BCK.
8	SCK	System clock output terminal. The output clock is obtained by 1/4 division of the X'tal oscillation output, and can be used as the system clock of signal processor circuitry. SCK = 16.9344MHz when X'tal = 67.7376MHz.
9	GND	ECL grounding terminal.
10	XO	Oscillator circuit input/output terminals.
11	XP	A modified Colpitts oscillator circuit is formed by combining L, C and R with as SAWE or X'tal oscillator.
12	XN	
13	VCCE	ECL logic power supply voltage terminal. (+5V)
14, 15	VEEA	Analog circuitry negative power supply voltage terminal. (–5V)
16	RSO	R ch sample & hold amplifier output terminal.
17	RSI	R ch sample & hold amplifier negative-input terminal.
18	OSR	R ch output offset adjustment terminal. Normally connected to GND A.
19	RIO	R ch integrating amplifier output terminal.
20	RII	R ch integrating amplifier negative-input terminal.
21	VDC	Charger circuit reference voltage terminal.
22	IADJ	Current source fine-adjustment terminal. Normally connected to GND A.
23	IREF	Reference current input terminal. IREF (recommended value) = 0.5mA.
24	GND S	Grounding terminal.
25	GND A	Analog grounding terminal.
26	LII	L ch integrating amplifier negative-input terminal.
27	LIO	L ch integrating amplifier output terminal.
28	OSL	L ch output offset adjustment terminal. Normally connected to GND A.
29	LSI	L ch sample & hold amplifier negative-input terminal.
30	LSO	L ch sample & hold amplifier output terminal.

Table 8–1

8–4. Explanation of function

● **Integration circuit and sampling holding circuit**

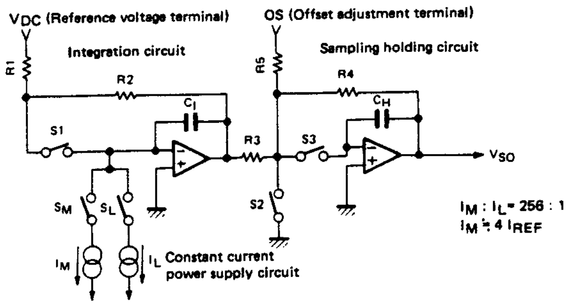


Fig. 8–3 Basic composition of integration circuit and sampling holding circuit

CIRCUIT DESCRIPTION

● **Basic operations of D/A conversion**

Step	S1	S2	S3	SM	SL	Contents of Operation
1	OFF	ON	OFF	ON/ OFF	ON/ OFF	(charging) integration operation = (Count – Voltage) conversion Sets S1 to OFF in order to charge C_I with two constant current supplies I_M and I_L. → D/A conversion of 16-bit digital data.
2	OFF	OFF	ON	OFF	OFF	(Sampling) Sets S1 to OFF and S3 to ON in order to charge the potential charged in C_I into C_H.
3	OFF	OFF	OFF	OFF	OFF	(Hold) Holds the potential charged in C_H at the moment immediately before S3 is set to OFF (S2 to ON).
4	ON	ON	OFF	OFF	OFF	(Discharging) reset operation Sets S1 in order to discharge the potential charged in C_I until it becomes equal to the reference voltage V_{RS}. $V_{RS} = -(R2/R1) \times V_{DC} = -(4k\Omega/6k\Omega) \times 5 = -3.3V$

Table 8–2

● **Timing chart**

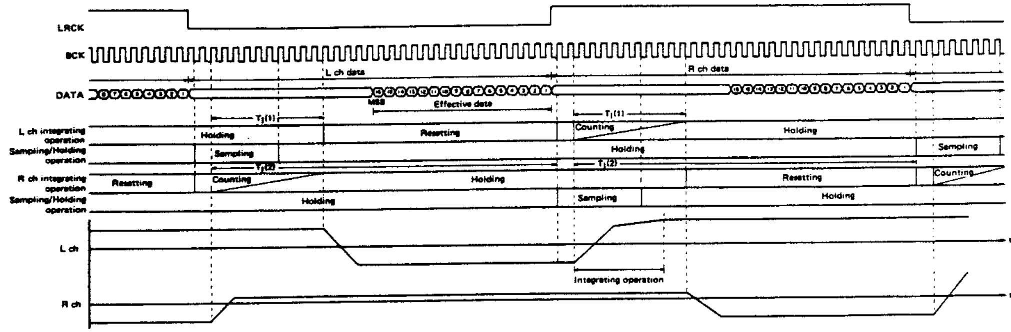
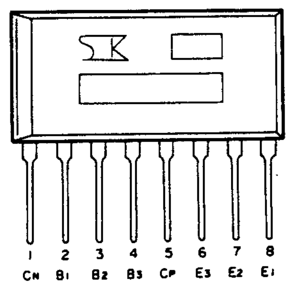


Fig. 8–4 Timing chart in case $f_{BCK} = 64f_{LR}$

9. Driver STA341M (X32-1260-23, X32-1262-73 : Q5) Japan made (X32-1302-72 : Q5) Singapore made

9–1. Terminal connection diagram



E : Emitter
B : Base
C : Collector

Fig. 9–1

9–2. Equivalent circuit

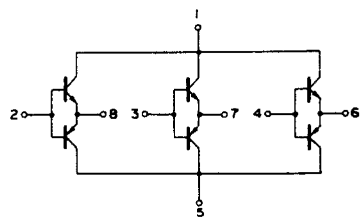


Fig. 9–2

MECHANISM OPERATION DESCRIPTION (X92-1300-00) JAPAN MADE

Mechanism Operation Description

Fig. 1 shows the relationship of mechanisms in the STOP mode. The OPEN/CLOSE operation of the mechanism and the UP/DOWN operation of the pickup chassis when loading the disc are description below.

Note 1 : The black arrow (OPEN) and the white arrow (CLOSE) in the operation description have the following meanings :

Black arrow (OPEN) : Tray opening direction (Tray OPEN)

White arrow (CLOSE) : Tray closing direction (Tray CLOSE)

Note 2 : Figures in the bracket ( ) in the operation description or accompanied with the part name in the diagram show the reference numbers in the Exploded View.

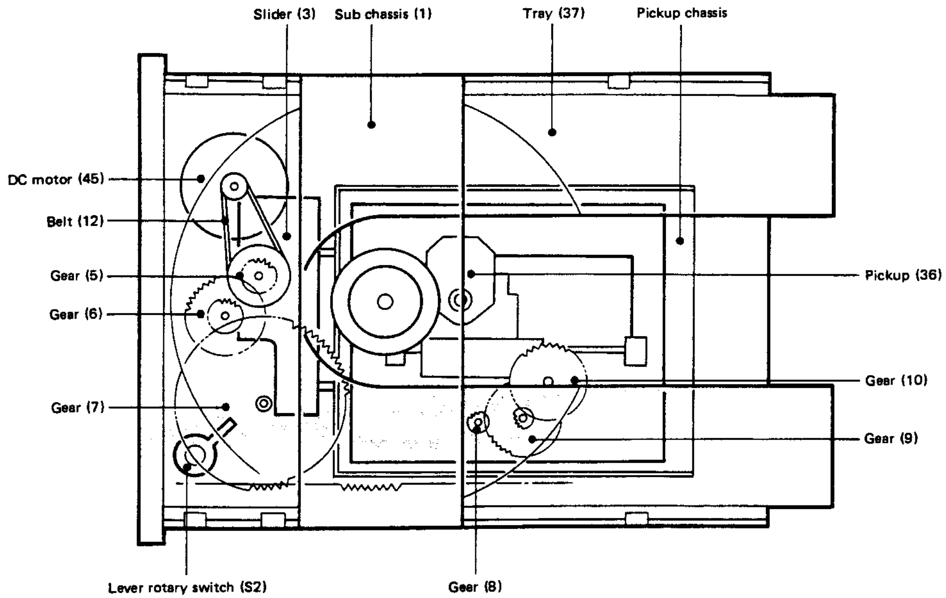


Fig. 1 Tray closed status

MECHANISM OPERATION DESCRIPTION (X92-1300-00) JAPAN MADE

1. Tray OPEN/CLOSE Operation

By the rotation of the motor (❶), the gear (❷) is rotated and the tray starts OPEN/CLOSE (❸) operation. The OPEN/CLOSE operation stops when the protrusion of the gear comes in contact with the detection switch (❹).

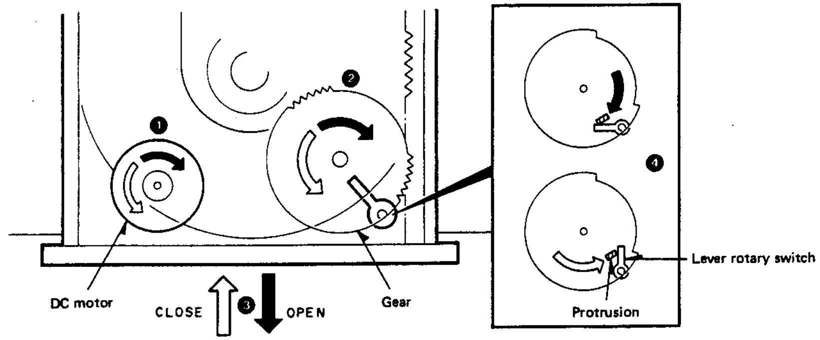


Fig. 2 Tray OPEN/CLOSE operation

2. Pickup Chassis UP/DOWN Movement

Accompanied with the OPEN/CLOSE operation, the lever is shifted (❷) by the rotation of the gear (❶). Along with the grooves in the lever, the pickup chassis moves up and down (❸).

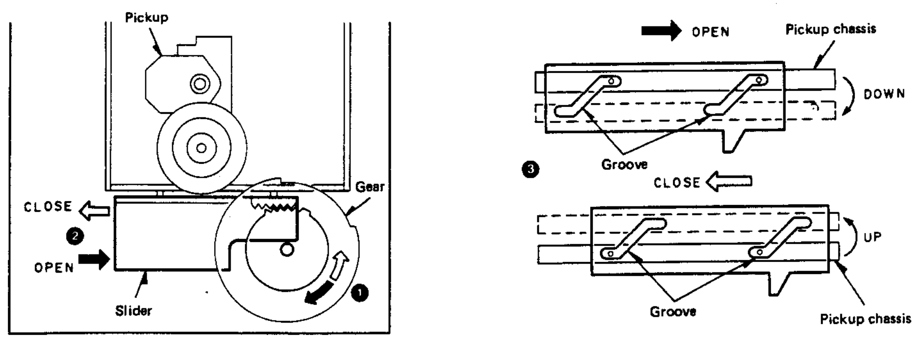


Fig. 3 Pickup chassis UP/DOWN movement

MECHANISM OPERATION DESCRIPTION (X92-1300-00)
JAPAN MADE

3. Gear Installing Position

When re-installing the gear after removing it, attach the gear at the position (A) shown in the condition when the pickup chassis has been lowered.

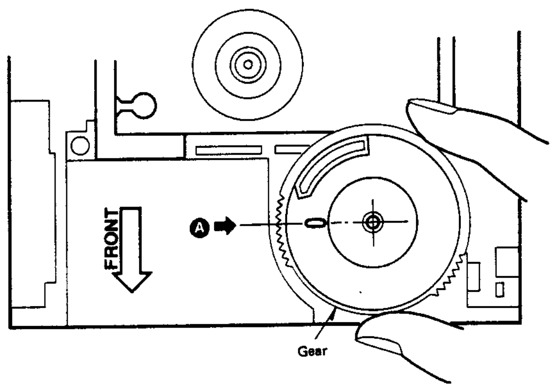


Fig. 4 Gear installing position

MECHANISM OPERATION DESCRIPTION (X92-1340-00)
SINGAPORE MADE

Mechanism Operation Description

Fig. 1 shows the relationship of mechanisms in the STOP mode. The OPEN/CLOSE operation of the mechanism and the UP/DOWN operation of the pickup chassis when loading the disc are described below.

Note 1 : The black arrow (OPEN) and the white arrow (CLOSE) in the operation description have the following meanings :

Black arrow (OPEN) : Tray opening direction (Tray OPEN)

White arrow (CLOSE) : Tray closing direction (Tray CLOSE)

Note 2 : Figures in the bracket ( ) in the operation description or accompanied with the part name in the diagram show the reference numbers in the Exploded View.

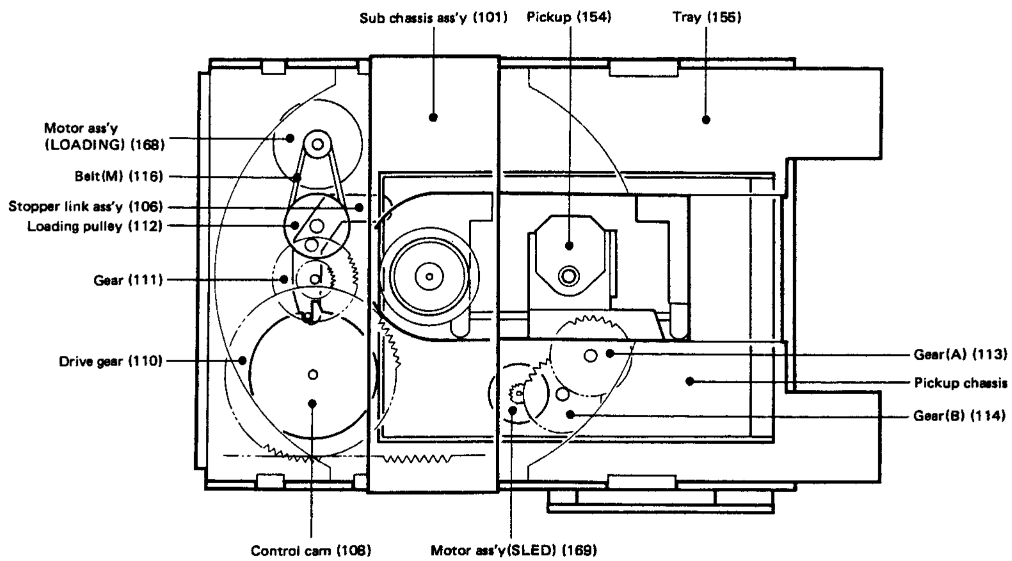


Fig. 1 Tray closed status

MECHANISM OPERATION DESCRIPTION (X92-1340-00) SINGAPORE MADE

1. Tray OPEN/CLOSE Operation

By the rotation of the DC motor (1), the drive gear (2) is rotated to provide the tray OPEN/CLOSE operation (3).

The tray OPEN/CLOSE operation stops when the protrusion of the drive gear comes into contact with the leaf switch (4).

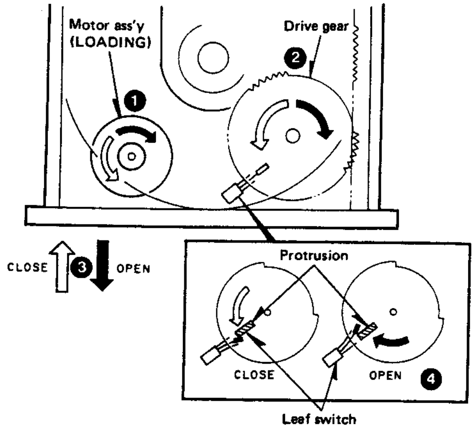


Fig. 2 Tray OPEN/CLOSE operation

2. Pickup Chassis UP/DOWN Movement

The control cam attached coaxially with the drive gear rotates in response to the tray OPEN/CLOSE operation (5). By this rotation, the protrusion of the pickup chassis moves along the groove of the control cam (6) so that the pickup chassis moves UP and DOWN correspondingly(7).

When the pickup chassis ascends fully by the rotation of the control cam in the UP (CLOSE) direction (8), the pickup chassis is locked by the lever (9).

When the control cam rotates in the DOWN (OPEN) direction (10), the pickup chassis is unlocked (11).

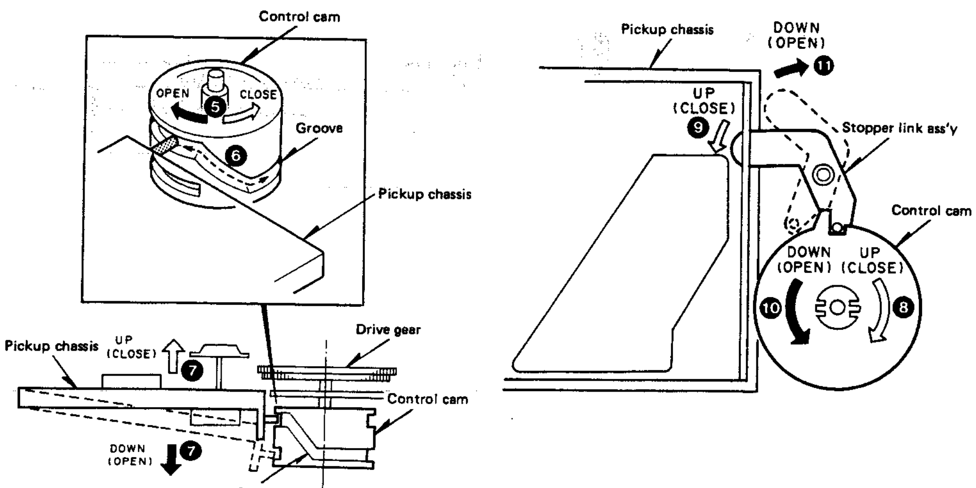


Fig. 3 Pickup chassis UP/DOWN movement

ADJUSTMENT

No.	ITEM	INPUT SETTING	OUTPUT SETTING	PLAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG
1	LASER POWER	–	Apply the sensor section of the optical power meter on the pickup lens.	Short-circuit pins TEST and turn power on to enter the Test mode. Press the MANUAL S. key(▶▶)to move the picup to the outermost position. Press the CHECK key, the LD should emit light. Check that the display is "03".	–	When the power is from 0.1 to 0.3mW, RF level is 1.5Vp-p or more, TE(servo open) is 1.5Vp-p or more and the diffraction grating is aligned correctly, the pickup is acceptable.	(a)
2	VCO	–	Connect a frequency counter to pin 8(PLCK) (X32-126/130)	Press the STOP key, and confirm that the display is "01".	L1 (X32-126/130)	4.32MHz	(b)
3	TRACKING ERROR BALANCE	Test disk Type 4	Connect an oscilloscope as follows. CH1: RF (X29-1890 pin 1) CH2: TE (X32-126/130 pin 6)	Press the REPEAT key to open the disc tray. Place the disc on the disc tray and push the tray to close it. Press the CHECK key and confirm that the display is"03".	TE BALANCE VR2 (X29-1890)	Symmetry between upper and lower patterns, or DC=0±0.05V	(c)
4	FOCUS ERROR BALANCE	Test disk Type 4	Connect an oscilloscope as follows. CH1: RF (X29-1890 pin 1) CH2: TE (X32-126/130 pin 6)	Press the PLAY Key, and confirm that the display is "05".	FE BALANCE VR1 (X29-1890)	Optimum eye pattern	(d)
5	FOCUS GAIN	Test disc Type 4 Apply 1kHz, 0.5Vrms signal to CN2 pin 2 of PC board (X32-126/130)	Use a servo jig, or connect an oscilloscope or AC voltmeter to pin 1 of CN2 via a 47kΩ, 470 pF LPF.(X32-126/130)	Press the PLAY Key, and confirm that the display is "05".	FOCUS GAIN VR1 (X32-126/130)	50mVrms	(e)
6	TRACKING GAIN	Test disc Type 4 Apply 1kHz, 0.5Vrms signal to CN2 pin 4 of PC board (X32-126/130)	Use a servo jig, or connect an oscilloscope or AC voltmeter to pin 5 of CN2 via a 47kΩ, 470 pF LPF.(X32-126/130)	Press the PLAY Key, and confirm that the display is "05".	TRACKING GAIN VR2 (X32-126/130)	50mVrms	(e)

(Note) Type 4 disk: SONY YEDS-18 Test Disk or equivalent.

REGLAGE

N°	ITEM	REGLAGE D'ENTREE	REGLAGE DE SORTIE	REGLAGE DE LA LECTURE	POINT D'ALIGNEMENT	ALIGNEMENT POUR	FIG
1	PUISSANCE LASER	–	Appliquer la section détecteur du compteur de puissance optique sur la lentille du capteur.	Court-circuiter les broches TEST et mettre l'alimentation en circuit pour entrer en mode de test. Presser la touche MANUAL S. (▶▶) pour déplacer le capteur jusqu'à la position la plus externe. Presser la touche CHECK. la diode devrait émettre de la lumière. Vérifier que l'affichage est " 03 ".	–	Quand l'alimentation est de 0,1 à 0,3mW, le niveau RF de 1,5Vc-c ou plus, TE (asservissement ouvert) de 1,5Vc-c ou plus et le réseau de diffraction aligné correctement, le capteur est acceptable.	(a)
2	VCO	–	Raccorder un compteur de fréquence à broche 8 (PLCK). (X32-126/130)	Presser la touche STOP et s'assurer que l'affichage est " 01 ".	L1 (X32-126/130)	4,32MHz	(b)
3	BALANCE D'ERREUR D'ALIGNEMENT	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1: RF (X29-1890 broche 1) CH2: TE (X32-126/130 broche 6)	Presser la touche REPEAT pour ouvrir le tiroir du disc. Placer le disc sur le tiroir et appuyer sur celui-ci pour le fermer. Presser la touche CHECK et s'assurer que l'affichage est " 03 ".	TE BALANCE VR2 (X29-1980)	Symétrie entre les formes supérieure et inférieure ou DC=0±0,05V	(c)
4	BALANCE D'ERREUR DE MISE AU POINT	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1: RF (X29-1890 broche 1) CH2: TE (X32-126/130 broche 6)	Presser la touche PLAY et s'assurer que l'affichage est " 05 ".	FE BALANCE VR1 (X29-1890)	Forme optimum	(d)
5	GAIN DE MISE AU POINT	Disque test Type 4 Appliguer un signal 1kHz, 0,5Vrms à la troche 2 de CN2 sur la plaquette X32-126/130.	Utiliser un gabarit d'asservissement ou raccorder un oscilloscope ou un voltmètre CC à la broche 1 de CN2 via un FPB de 47kΩ, 470 pF.	Presser la touche PLAY et s'assurer que l'affichage est " 05 ".	GAIN DE MISE AU POINT VR1 (X32-126/130)	50mVrms	(e)
6	GAIN D'ALIGNMENT	Disque test Type 4 Appliguer un signal 1kHz, 0,5Vrms à la troche 4 de CN2 sur la plaquette X32-126/130.	Utiliser un gabarit d'asservisement ou raccorder un oscilloscope ou un voltmètre CC à la broche 5 de CN2 via un FPB de 47kΩ, 470 pF.	Presser la touche PLAY et s'assurer que l'affichage est " 05 ".	GAIN D'ALIGNEMENT VR2 (X32-126/130)	50mVrms	(e)

(Remarque)Disque de type 4:Disque test SONY YEDS-18 ou équivalent.

ABGLEICH

NR.	GEGENSTAND	EINGANGS-EINSTELLUN	AUSGANGS-EINSTELLUNGE	SPIELER-EINSTELLUNG	ABGLEICH-PUNKT	ABGLEICHUNG	ABB.
1	LASERLEISTUNG	–	Das Sensorteil des optischen Leistungmeters auf die Aufnehmerlinse ansetzen.	Die Stifte TEST kurzschließen und die Spannungsversorgung einschalten, um den Test-Modus zu aktivieren. Die Taste MANUAL S. (▶▶) drücken, um den Abnehmer ganz nach außen zu bringen. Die Taste CHECK drücken, dann muß die LD Licht abstrahlen. Prüfen, daß " 03 " angezeigt wird.	–	Wenn bei einer Spannung von 0,1 bis 0,3 mW der RF-Pegel 1,5Vs-s oder mehr, TE (Servo-Offen) 1,5Vs-s beträgt und das Beugungsgitter richtig ausgerichtet ist, ist der Abtaster in Ordnung.	(a)
2	VCO	–	Einen Frequenzzähler an Stift 8(PLCK) anschließen. (X32-126/130)	Die STOP-Taste drücken und prüfen, daß " 01 " auf dem Display angezeigt wird.	L1 (X32-126/130)	4,32MHz	(b)
3	SPURHALTEFEHLER-AUSGLEICH	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1: RF (X29-1890 Stift 1) Kanal 2: TE (X32-126/130 Stift 6)	Die REPEAT-Taste drücken, um den Disc-Träger zu öffnen. Die Disc auf den Disc-Träger legen und gegen den Träger drücken, um ihn zu schließen. Die CHECK-Taste drücken und prüfen, daß " 03 " auf dem Display angezeigt wird.	TE BALANCE VR2 (X29-1980)	Symmetrie zwischen oberen und unteren Mustern oder Gleichstrom DC=0±0,05V	(c)
4	FOKUS-FEHLERAUSGLEICH	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1: RF (X29-1890 Stift 1) Kanal 2: TE (X32-126/130 Stift 6)	Die CHECK-Taste drücken und prüfen, daß " 05 " auf dem Display angezeigt wird.	FOKUS-FEHLERAUSGLEICH VR1 (X29-1890)	Optimales Augenmuster	(d)
5	FOKUSVERSTÄRKUNG	Testdisc Typ 4 Ein 1kHz, 0,5Vrms Signal an Stift 2 von CN2 an platine X32-126/130 anlegen.	Eine Servo-Lehre verwenden oder ein Oszilloskop oder einen Wechselstrom-Voltmeter an Stift 1 von CN2 über ein 47kΩ, 470pF Tiefpaßfilter anschließen.	Die CHECK-Taste drücken und prüfen, daß " 05 " auf dem Display angezeigt wird.	FOKUSVERSTÄRKUNG VR1 (X32-126/130)	50mVrms	(e)
6	SPURHALTE-VERSTÄRKUNG	Testdisc Typ 4 Ein 1kHz, 0,5Vrms Signal an Stift 4 von CN2 an platine X32-126/130 anlegen.	Eine Servo-Lehre verwenden oder ein Oszilloskop oder einen Wechselstrom-Voltmeter an Stift 5 von CN2 über ein 47kΩ, 470pF Tiefpaßfilter anschließen.	Die CHECK-Taste drücken und prüfen, daß " 05 " auf dem Display angezeigt wird.	SPUHALTE-VERSTÄRKUNG VR2 (X32-126/130)	50mVrms	(e)

(Hinweis) Typ 4 Disc: SONY YEDS-18 Testdisc oder Äquivalent.

ADJUSTMENT/REGLAGE/ABGLEICH

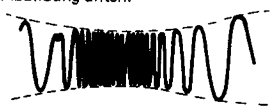
DIFFRACTION GRID ADJUSTMENT/REGLAGE DU RESEAU DE DIFFRACTION/BEUGUNGSGITTER-EINSTELLUNG

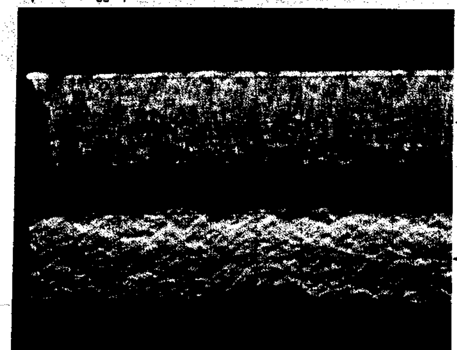
(Photo. 1)
(Photo. 1)
(Foto. 1)

- RF signal and T.Error signal after diffraction grating adjustment.
- Signal RF et signal T.Error après ajustement de réseau de diffraction.
- RF-Signal und T.Error-Signal nach Diffraktions-gitter-Einstellung.

(Photo. 2)
(Photo. 2)
(Foto. 2)

- RF signal and T.Error signal when there is small diffraction grating position error.
- The T.Error signal level is small, and the envelope is as shown in the diagram below.
- Signal RF et signal T.Error quand il y a une petite erreur de position du réseau de diffraction.
- Le niveau de signal T.Error est petit et l'envelope est telle qu'indiquée dans le diagramme ci-dessous.
- RF-Signal und T.Error-Signal bei kleinem Diffraktions-gitter-Positionierungsfehler.
- Der T.Error-Signalpegel ist klein, und die Hüll-kurve ist wie in der Abbildung unten.

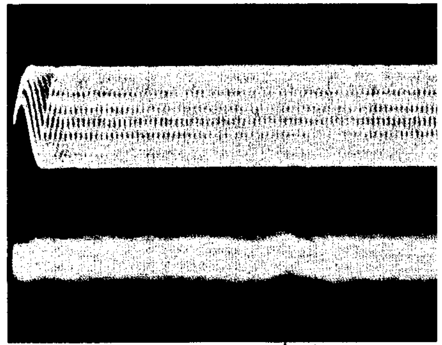




(Photo. 3)
(Photo. 3)
(Foto. 3)

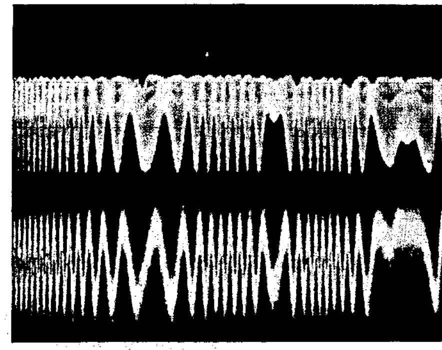
- RF signal and T.Error signal in test mode (with focusing ON).
- When the sub-beam traces the same bit series as the main beam during diffraction grating adjustment, bringing the RF trigger point to the position shown in the Photo causes a "projection" to be observies in the T.Error waveform.
- Le signal RF et le signal T.Error en mode de test (avec la mise au point sur ON).
- Quand un faisceau auxiliaire tracela même série de bits que le faisceau principal pendant l'ajustement de réseau de diffraction, l'apport du point de déclenchement RF à la position indiquée dans la photo provoque une "projection" qui s'observe dans la forme d'onde d' T.Error.
- RF-Signal und T.Error-Signal im Testmodus (bei eingeschalteter Fokussierung).
- Wenn der Nebenstrahl die gleiche Bitreihe wie der Hauptstrahl während der Diffraktionsgitter-Einstellung verfolgt und den RF-Triggerpunkt auf die im Foto gezeigte Position bringt, wird eine "Hervorstehung" verursacht, die in der T.Error-Wellenform beobachtet werden kann.

ADJUSTMENT/REGLAGE/ABGLEICH



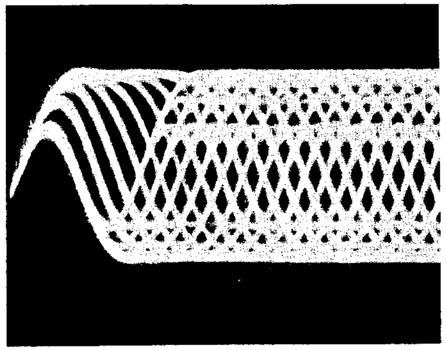
(Photo. 4)
(Photo. 4)
(Foto. 4)

- RF signal and E.Spot signal in test mode (PLAY).
- If the diffraction grating has been adjusted properly, the influence of triggering is observed on the E.Spot waveform of approx. 12μs after RF signal, in the form of a projection.
- Signal RF et signal E.Spot en mode de test (PLAY).
- Si le réseau de diffraction a été ajusté correctement, l'influence du déclenchement s'observe sur la forme d'onde E.Spot d'environ 12μs après le signal RF, sous la forme d'une projection.
- RF-Signal und E.Spot-Signal im Testmodus (PLAY).
- Wenn das Diffraktionsgitter richtig eingestellt wurde, wird der Einfluß des Triggers in der E.Spot-Wellenform etwa 12μs nach dem RF-Signal in der Form einer Hervorstehung beobachtet.



(Photo. 5)
(Photo. 5)
(Foto. 5)

- RF signal and T.Error signal; in test mode (Focusing ON). (Disc type 4)
- Adjust T.Error so that the waveform is symmetrical above and below 0V. (VR1 of X29-1890)
- Signal RF et signal T.Error; en mode test (mise au point ON). (Disque de type 4)
- Ajuster T.Error pour que la forme d'onde soit symétrique en-dessus et au-dessous de 0V. (VR1 de X29-1980)
- RF-Signal und T.Error-Signal; im Testmodus (Fokussierung eingeschaltet). (Disc-Typ 4)
- T.Error so einstellen, daß die Wellenform über und unter 0V symmetrisch ist. (VR1 von X29-1890)

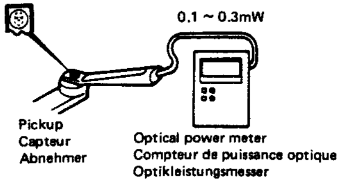


(Photo. 6)
(Photo. 6)
(Foto. 6)

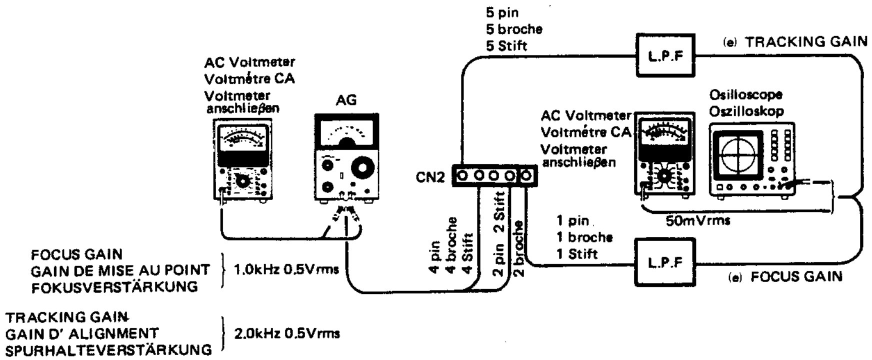
- RF signal in test mode (PLAY).
- Perform the tangential and focusing offset adjustments so that each of the center cross points are focused into one point on the display. The crossing points above and below the center shall also be displayed clearly.
- Signal RF en mode de test (PLAY).
- Effectuer les ajustements d'offset tangentiel et de mise au point pour que chacun des points de croisement central soit mis au point sur un point de l'affichage. Les points de croisement au-dessus et en-dessous du centre doivent aussi être affichés clairement.
- RF-Signal im Testmodus (PLAY).
- Die Tangential- und Fokusversatz-Einstellungen so durchführen, daß jeder der mittleren Kreuzungspunkte in einem Punkt auf dem Display fokussiert wird. Auch die Kreuzungspunkte über und unter der Mitte müssen klar angezeigt werden.

ADJUSTMENT/REGLAGE/ABGLEICH

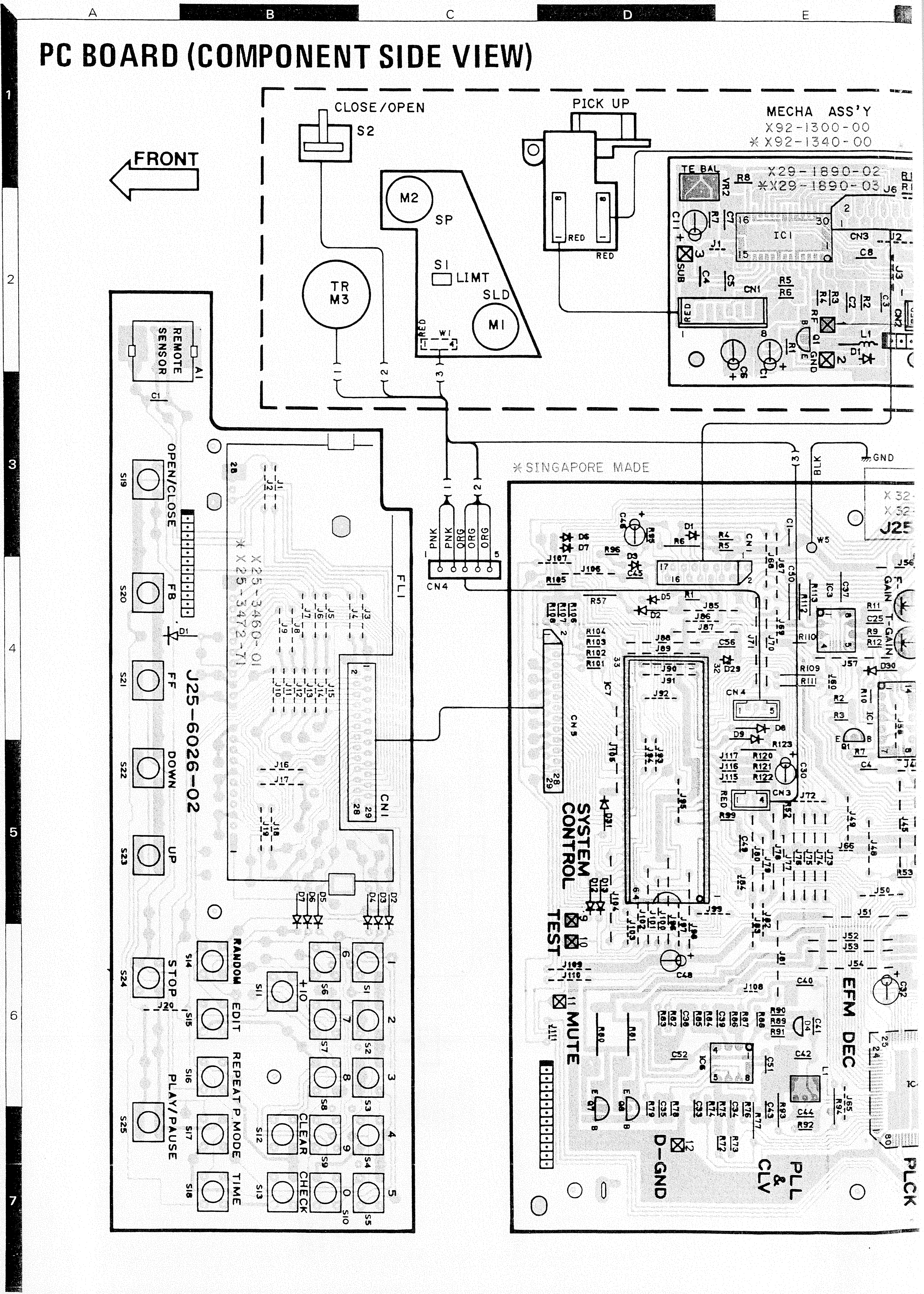
(a) Laser Power

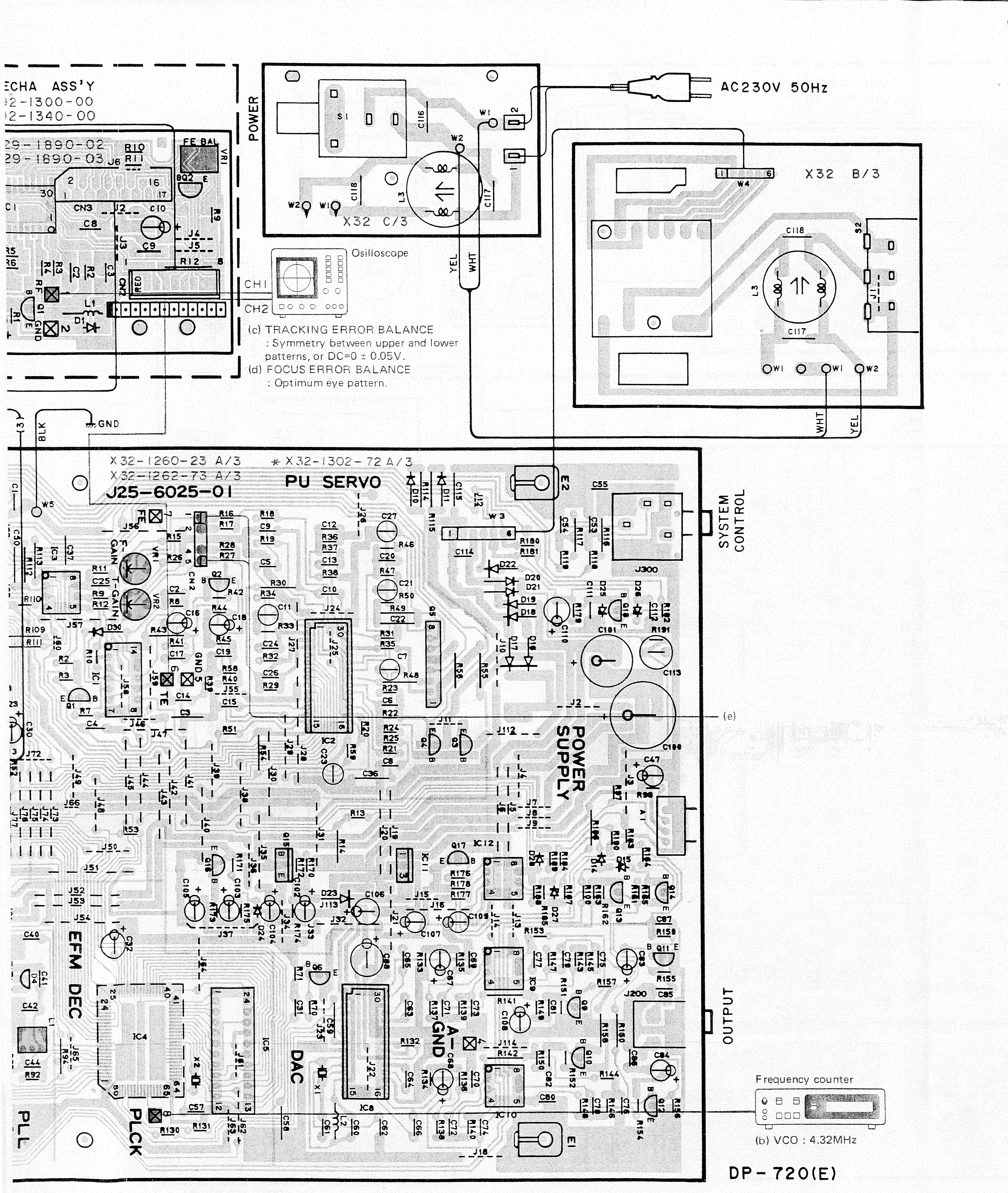


(e) Focus Gain, Tracking Gain



PC BOARD (COMPONENT SIDE VIEW)





Refer to the schematic diagram for the values of resistors and capacitors.

(X32-XXXX-XX)

IC1

1 ~ 4	0V
5	5.0V
6	4.0V
7	−5.0V
10, 11	0V
12, 13	4.7V
14	5.0V

IC2

1 ~ 5	0V
6	1.6V
7	4.8V
8 ~ 10	5.0V
11	1.2V
12, 13	0V
14	−4.3V
15	5.0V
16	0V
17	−5.0V
18	−4.4V
19	0V
20	−0.2V
21	−0.7V
22	0V
23	0.6V
24, 25	0V
26	5.0V
27	0.5V
28 ~ 30	0V

IC3

1	0.5V
2, 3	0V
4	−10.0V
5 ~ 7	0V
8	10.0V

IC4

1 ~ 4	0V
5	4.2V
6	2.1V
8, 9	2.5V
10	0V
11	2.5V
12	0V
13 ~ 15	5.0V
16	4.8V
17	1.6V
18	0V
19	5.0V
20, 23, 24	0V
25	2.5V
26, 28	0V
29 ~ 31	0.7V
32	2.8V
33	5.0V
34, 35	2.8V
36	2.3V
37	4.5V
38 ~ 45	2.5V
46	2.4V
47 ~ 49	2.5V
50	2.2V
51	1.6V
52	0V
53	2.5V
54	2.6V
55	0V
56	5.0V
57 ~ 59	0V
70	1.6V
73	5.0V
76	2.2V
78	0V
80	2.5V

IC5

1 ~ 7	2.5V
8	2.3V
9, 10	2.8V
11	0.7V
12	0V
13, 14	0.7V
15	2.8V
16	2.3V
17	4.5V
18	2.2V
19	2.4V
20	2.2V
21 ~ 23	2.5V
24	5.0V

IC6

1	0V
2, 3	2.5V
4	−10.0V
5, 6	0V
7	0.6V
8	10.0V

IC7

1 ~ 4	−11.3V
5	0V
6	2.5V
7, 8	0V
9	4.9V
10 ~ 13	0V
15, 16	5.0V
18	0V
19	5.0V
20 ~ 24	0V
25 ~ 28	5.0V
~30	1.7V
32, 33	0V
35 = 38	0V
39	4.8V
40 ~ 48	−25.8V
52	5.0V
53	0.2V
54	−18.3V
55	−11.3V
56	−30.0V
57	−5.0V
58	−22.0V
59	−18.4V
61	−14.5V
62, 63	−21.6V
64	5.0V

IC8

1, 2	5.0V
3	2.2V
4	5.0V
5	0V
7	2.5V
8	4.0V
9	0V
10	4.9V
11	2.9V
12	2.3V
13	5.0V
14, 15	−5.0V
16	−0.3V
17, 18	0V
19	−1.0V
20	0V
21	5.0V
22	0V
23	−3.7V
24 ~ 26	0V
27	−1.0V
28, 29	0V
30	−0.3V

IC9

1 ~ 3	0V
4	−10.0V
5 ~ 7	0V
8	10.0V

IC10

1 ~ 3	0V
4	−10.0V
5 ~ 7	0V
8	10.0V

IC11

I	10.0V
O	5.0V
G	0V

IC12

1	−5.6V
2, 3	0V
4	−10.0V
5	4.1V
6	3.5V
7	8.6V
8	10.0V

Q5

1	9.8V
2	0.5V
3	0.6V
4	0.5V
5	−9.8V
6 ~ 8	0V

	B	E	C
Q1	4.4V	5.0V	5.0V
Q2	0.6V	0V	2.0V
Q3	−0.7V	0V	10.0V
Q4	−0.7V	0V	−10.0V
Q6	0.6V	0V	1.6V
Q7	0.6V	0V	10.0V
Q8	0.6V	0V	−10.0V
Q9	0.7V	0V	0V
Q10	0.7V	0V	0V
Q11	0.7V	0V	0V
Q12	0.7V	0V	0V
Q13	4.3V	4.9V	5.0V
Q14	−5.0V	−5.0V	2.5V
Q15	5.6V	5.0V	10.0V
Q16	−5.6V	−5.0V	−10.0V
Q17	−5.6V	−5.0V	−10.0V
Q18	−29.2V	−30.0V	−39.5V
Q19	0.7V	0V	0V
Q20	0V	0V	0V

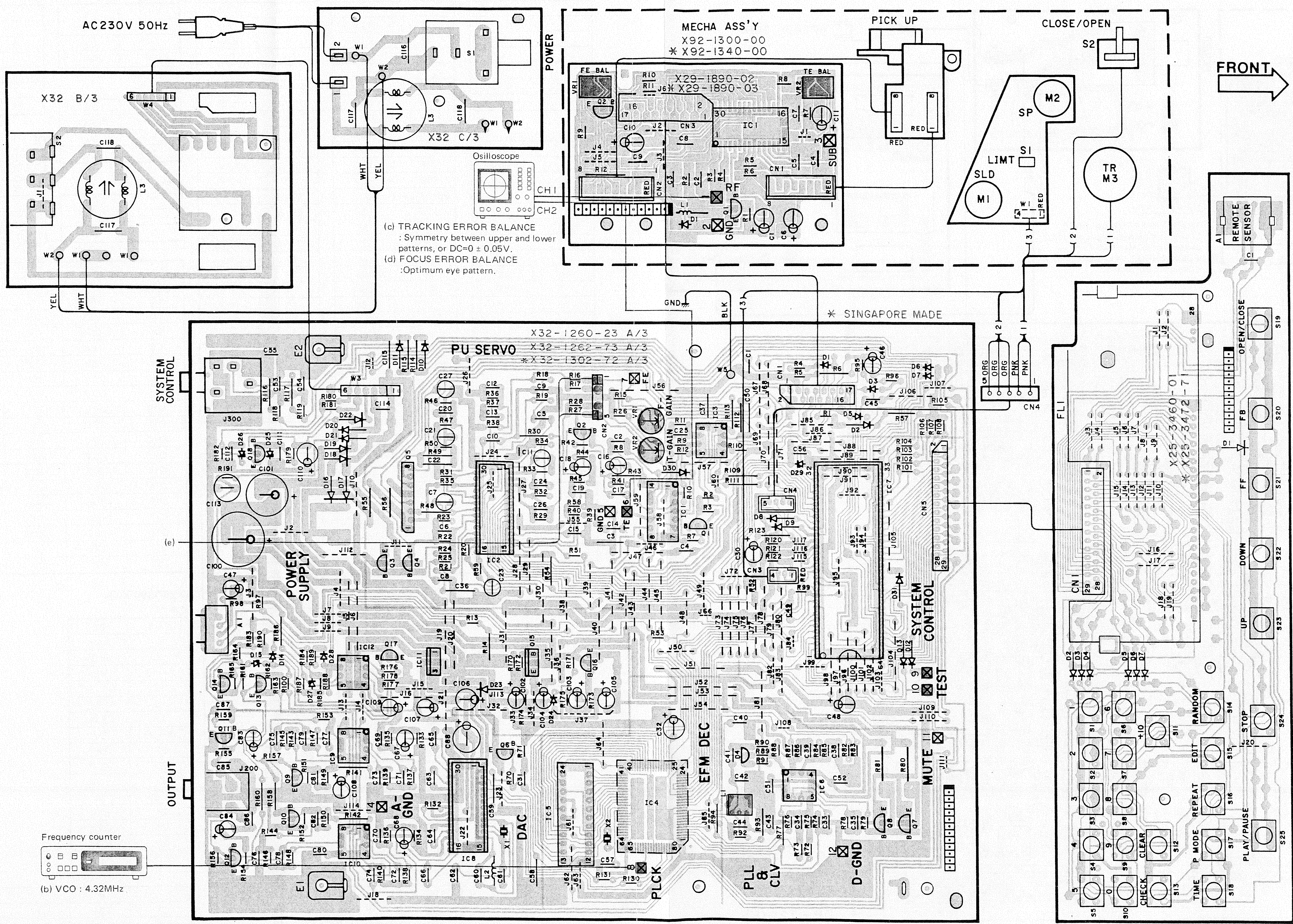
(X29-1890-XX)

IC1

1 ~ 3	0V
5	4.8V
6	−5.0V
7 ~ 13	0V
15	−1.0V
16	1.2V
17	−5.0V
18 ~ 20	0V
21	0.9V
22	−3.4V
23	3.8V
24, 25	0V
26	2.1V
27	4.2V
28	0.2V
29, 30	5.0V

	B	E	C
Q1	4.8V	5.0V	0.2V
Q2	0.6V	0V	0V

PC BOARD (FOIL SIDE VIEW)



Refer to the schematic diagram for the values of resistors and capacitors.

(X32-XXXX-XX)

IC1

1 ~ 4	0V
5	5.0V
6	4.0V
7	−5.0V
10, 11	0V
12, 13	4.7V
14	5.0V

IC2

1 ~ 5	0V
6	1.6V
7	4.8V
8 ~ 10	5.0V
11	1.2V
12, 13	0V
14	−4.3V
15	5.0V
16	0V
17	−5.0V
18	−4.4V
19	0V
20	−0.2V
21	−0.7V
22	0V
23	0.6V
24, 25	0V
26	5.0V
27	0.5V
28 ~ 30	0V

IC3

1	0.5V
2, 3	0V
4	−10.0V
5 ~ 7	0V
8	10.0V

IC4

1 ~ 4	0V
5	4.2V
6	2.1V
8, 9	2.5V
10	0V
11	2.5V
12	0V
13 ~ 15	5.0V
16	4.8V
17	1.6V
18	0V
19	5.0V
20, 23, 24	0V
25	2.5V
26, 28	0V
29 ~ 31	0.7V
32	2.8V
33	5.0V
34, 35	2.8V
36	2.3V
37	4.5V
38 ~ 45	2.5V
46	2.4V
47 ~ 49	2.5V
50	2.2V
51	1.6V
52	0V
53	2.5V
54	2.6V
55	0V
56	5.0V
57 ~ 59	0V
70	1.6V
73	5.0V
76	2.2V
78	0V
80	2.5V

IC5

1 ~ 7	2.5V
8	2.3V
9, 10	2.8V
11	0.7V
12	0V
13, 14	0.7V
15	2.8V
16	2.3V
17	4.5V
18	2.2V
19	2.4V
20	2.2V
21 ~ 23	2.5V
24	5.0V

IC6

1	0V
2, 3	2.5V
4	−10.0V
5, 6	0V
7	0.6V
8	10.0V

IC7

1 ~ 4	−11.3V
5	0V
6	2.5V
7, 8	0V
9	4.9V
10 ~ 13	0V
15, 16	5.0V
18	0V
19	5.0V
20 ~ 24	0V
25 ~ 28	5.0V
30	1.7V
32, 33	0V
35 ~ 38	0V
39	4.8V
40 ~ 48	−25.8V
52	5.0V
53	0.2V
54	−18.3V
55	−11.3V
56	−30.0V
57	−5.0V
58	−22.0V
59	−18.4V
61	−14.5V
62, 63	−21.6V
64	5.0V

IC8

1, 2	5.0V
3	2.2V
4	5.0V
5	0V
7	2.5V
8	4.0V
9	0V
10	4.9V
11	2.9V
12	2.3V
13	5.0V
14, 15	−5.0V
16	−0.3V
17, 18	0V
19	−1.0V
20	0V
21	5.0V
22	0V
23	−3.7V
24 ~ 26	0V
27	−1.0V
28, 29	0V
30	−0.3V

IC9

1 ~ 3	0V
4	−10.0V
5 ~ 7	0V
8	10.0V

IC10

1 ~ 3	0V
4	−10.0V
5 ~ 7	0V
8	10.0V

IC11

I	10.0V
O	5.0V
G	0V

IC12

1	−5.6V
2, 3	0V
4	−10.0V
5	4.1V
6	3.5V
7	8.6V
8	10.0V

Q5

1	9.8V
2	0.5V
3	0.6V
4	0.5V
5	−9.8V
6 ~ 8	0V

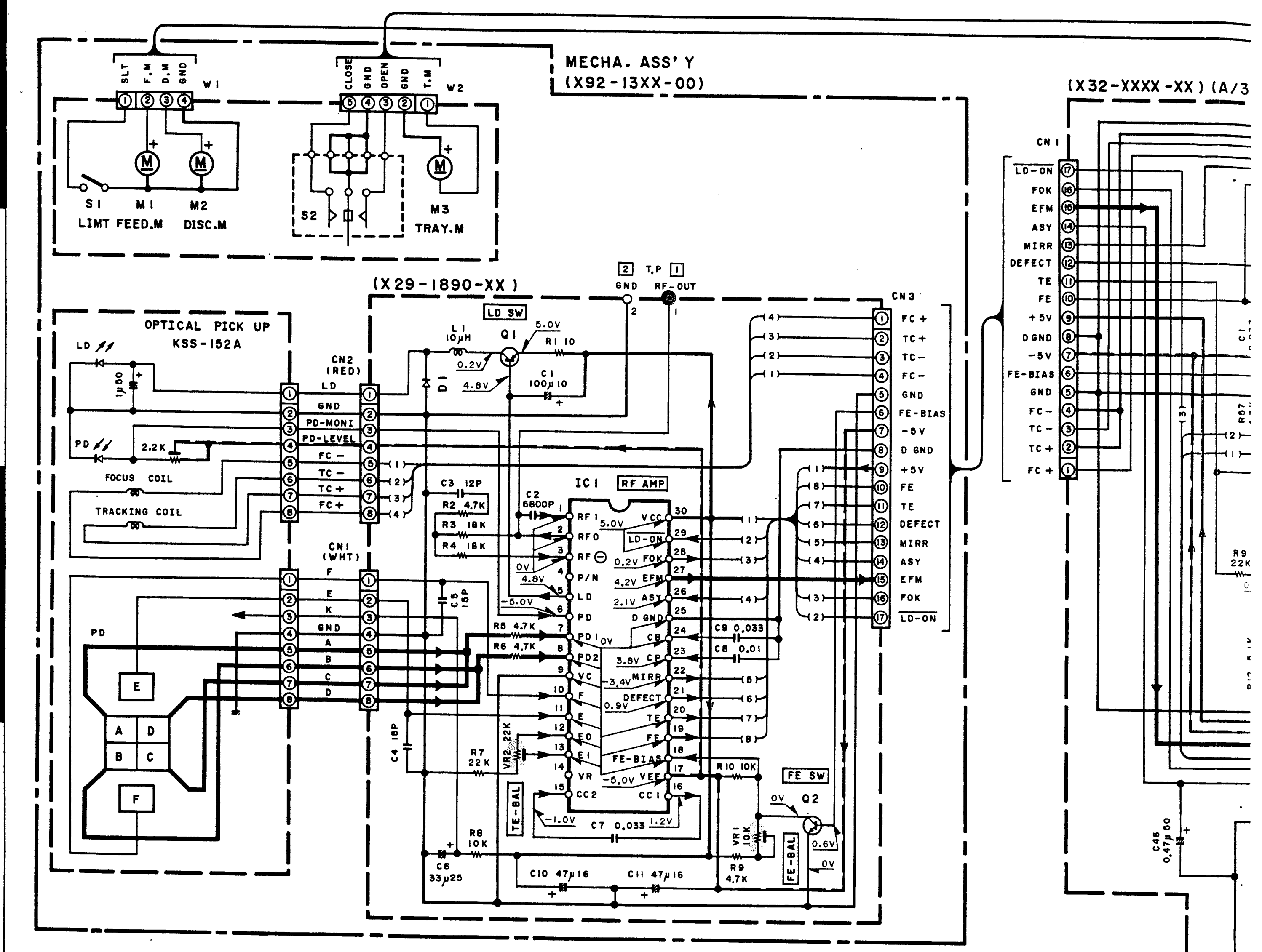
	B	E	C
Q1	4.4V	5.0V	5.0V
Q2	0.6V	0V	2.0V
Q3	−0.7V	0V	10.0V
Q4	−0.7V	0V	−10.0V
Q6	0.6V	0V	1.6V
Q7	0.6V	0V	10.0V
Q8	0.6V	0V	−10.0V
Q9	0.7V	0V	0V
Q10	0.7V	0V	0V
Q11	0.7V	0V	0V
Q12	0.7V	0V	0V
Q13	4.3V	4.9V	5.0V
Q14	−5.0V	−5.0V	2.5V
Q15	5.6V	5.0V	10.0V
Q16	−5.6V	−5.0V	−10.0V
Q17	−5.6V	−5.0V	−10.0V
Q18	−29.2V	−30.0V	−39.5V
Q19	0.7V	0V	0V
Q20	0V	0V	0V

(X29-1890-XX)

IC1

1 ~ 3	0V
5	4.8V
6	−5.0V
7 ~ 13	0V
15	−1.0V
16	1.2V
17	−5.0V
18 ~ 20	0V
21	0.9V
22	−3.4V
23	3.8V
24, 25	0V
26	2.1V
27	4.2V
28	0.2V
29, 30	5.0V

	B	E	C
Q1	4.8V	5.0V	0.2V
Q2	0.6V	0V	0V



(X32-XXXX-XX)

Ref. No. / DESTINATION	C6	C8	C11	C117, 118	C119, 120	L3	L4	R22	R23	R25	R41
X32-1260-23(M)	2200P	0.27	4.7μ25	YES	NO	YES	NO	150K	4.7K	82	47K
2-73(X,T,E)				NO	YES	NO	YES				
X32-1302-72(T,E)	1000P	0.18	4.7μ50	YES	NO	YES	NO	120K	11K	130	36K

Ref. No. / DESTINATION	R58	R59	R60	S2	D13,31
X32-1260-23(M)	100K	1.5M	18	YES	NO
2-73(X,T,E)				NO	
X32-1302-72(T,E)	47K	2.2M	J	YES	YES

(X29-1890-XX)

IC1 : CXA1081M

Q1 : 2SA1426
Q2 : 2SC945(A)(Q,P)

D1 : 1SS133 or 1SS176

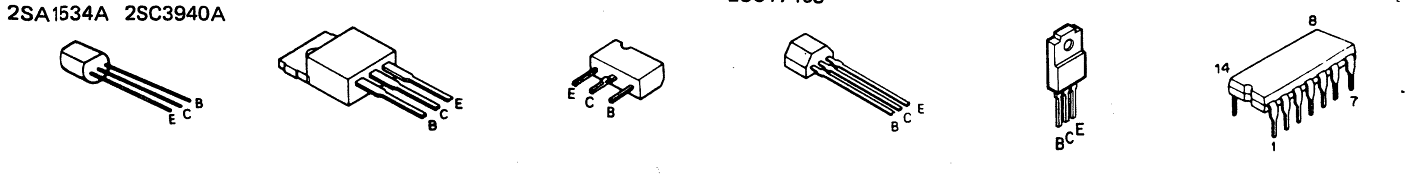
(X32-XXXX-XX)

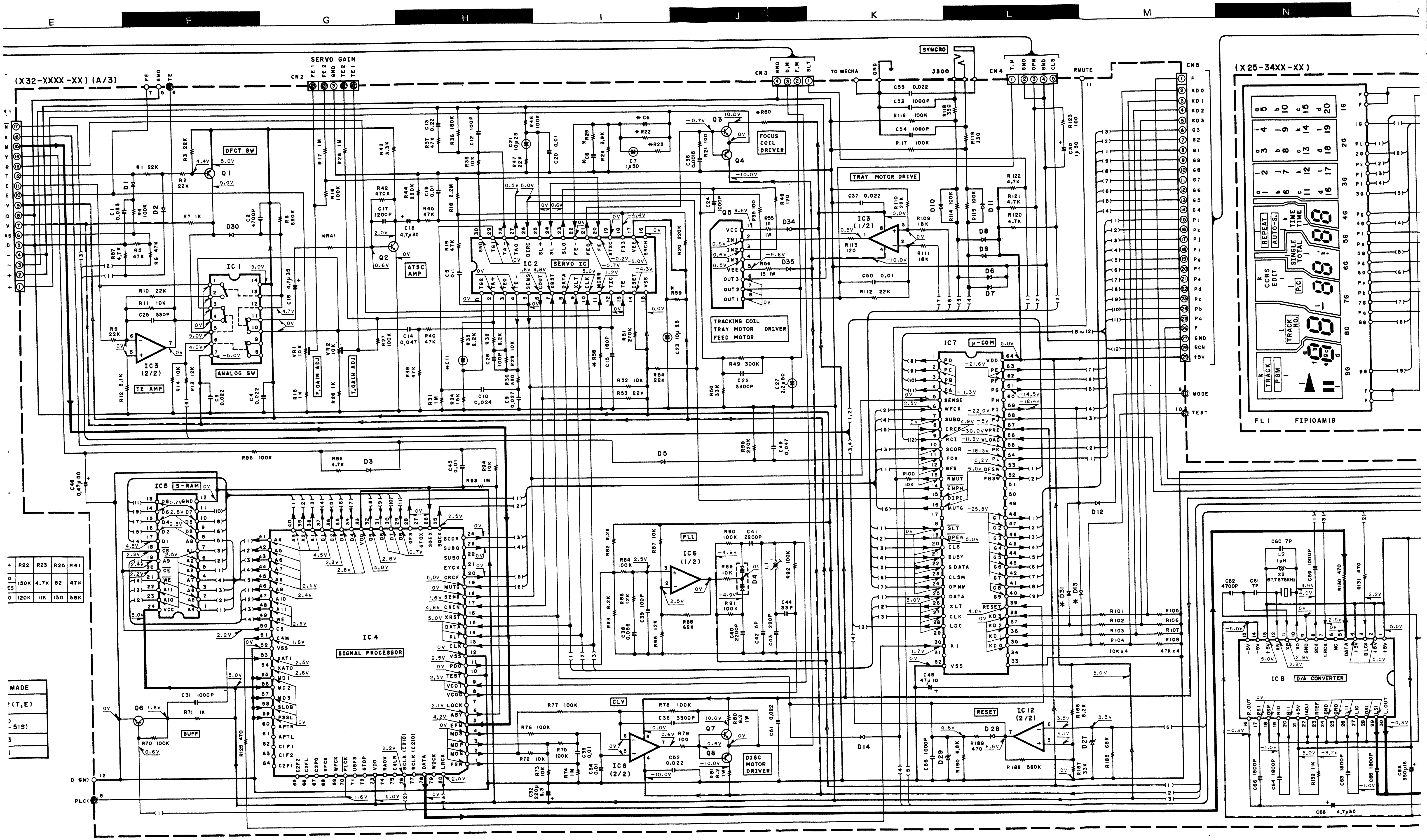
IC1 : TC4066BP
IC2 : CXA1244S
IC3,6,9,10,12 : M5218P
IC4 : CXD1135QZ or CXD1135Q
IC5 : LC3518BSL-15
IC7 : μPD75212ACW-028
IC8 : TD6720N
IC11 : LM2940CT-5.0

Q1,13 : 2SA733(A)(Q,P) or 2SA933S(Q,R)
Q2,6,14 : 2SC945(A)(Q,P) or 2SC1740S(Q,R)
Q3 : 2SD1266
Q4,8 : 2SA1534A
Q5 : STA341M
Q7 : 2SC3940A
Q9~12,19,20 : 2SC2878(B)
Q15 : 2SD1944
Q16~18 : 2SA954(L,K)
D1~3,5~11,14,20,21,23,24
28,30,32,33 : 1SS133 or HSS104
D4 : 1SV147
D12,13,31 : 1SS131 or HSS104A
D15 : RD8.2JS(B2) or HZS8.2S(B2)
D16~19,22,34,35: S5566B
D25 : RD30JS(B) or HZS30S(B)
D26 : RD5.6JS(B2) or HZS5.6S(B2)
D27 : RD3.3ES(B2) or HZS3.3N(B2)
D29 : RD4.7ES(B) or HZS4.7N(B)

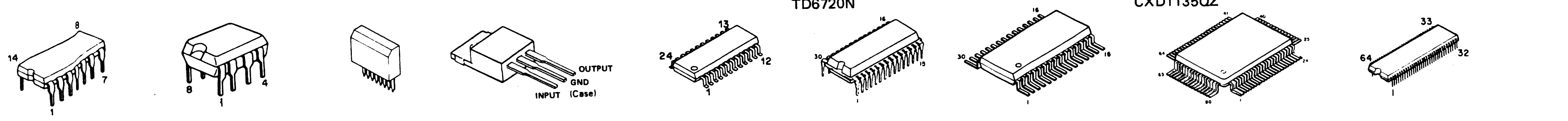
JAPAN MADE	SINGAPORE MADE
X32-1260-23 (M) 2-73(X,T,E)	X32-1302-72(T,E)
X92-1300-00 (CDM-13A)	X92-1340-00 (CDM-51S)
X29-1890-02	X29-1890-03
X25-3460-01	X25-3472-71

2SA733(A) 2SC945(A) 2SA954 2SC2878 2SA1534A 2SC3940A — 2SD1266 — 2SA1426 — 2SA933S 2SC1740S — 2SD1944 — TC4066BP

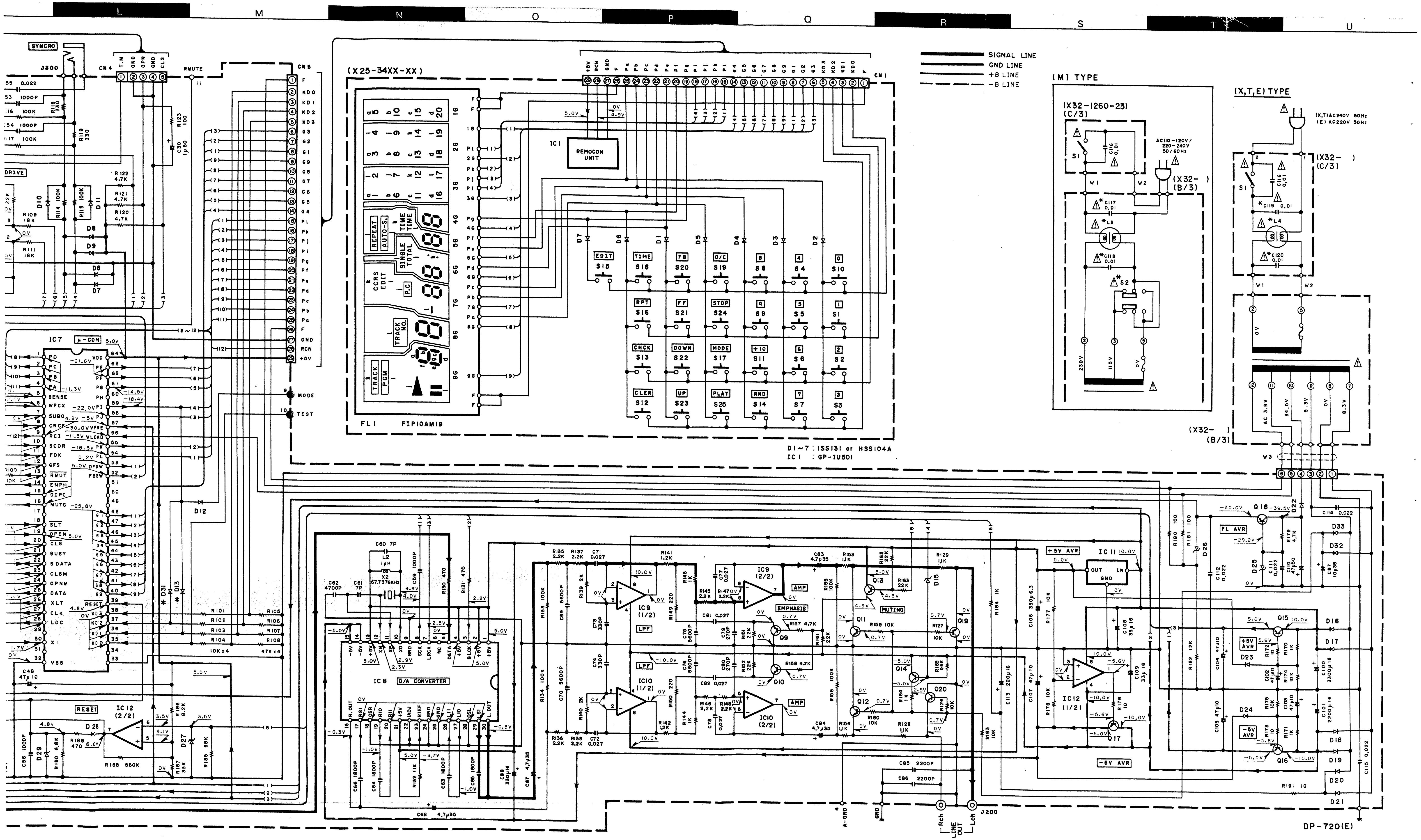




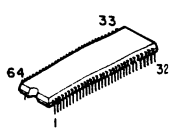
TC4066BP | M5218P | STA341M | LM2940CT-5.0 | LC3518BSL-15 | CXA1244S TD6720N | CXA1081M | CXD1135Q CXD1135QZ | μPD75212ACW-028



CAUTION: For continued safety, replace ponents only with manufacturer's recomm to parts list). ⚠Indicates safety critica reduce the risk of electric shock, leakage-c measurements shall be carried out (expose bly insulated from the supply circuit) bef returned to the customer.



µPD75212ACW-028



CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

- DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.
- Les tensions c.c. doivent être mesurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.

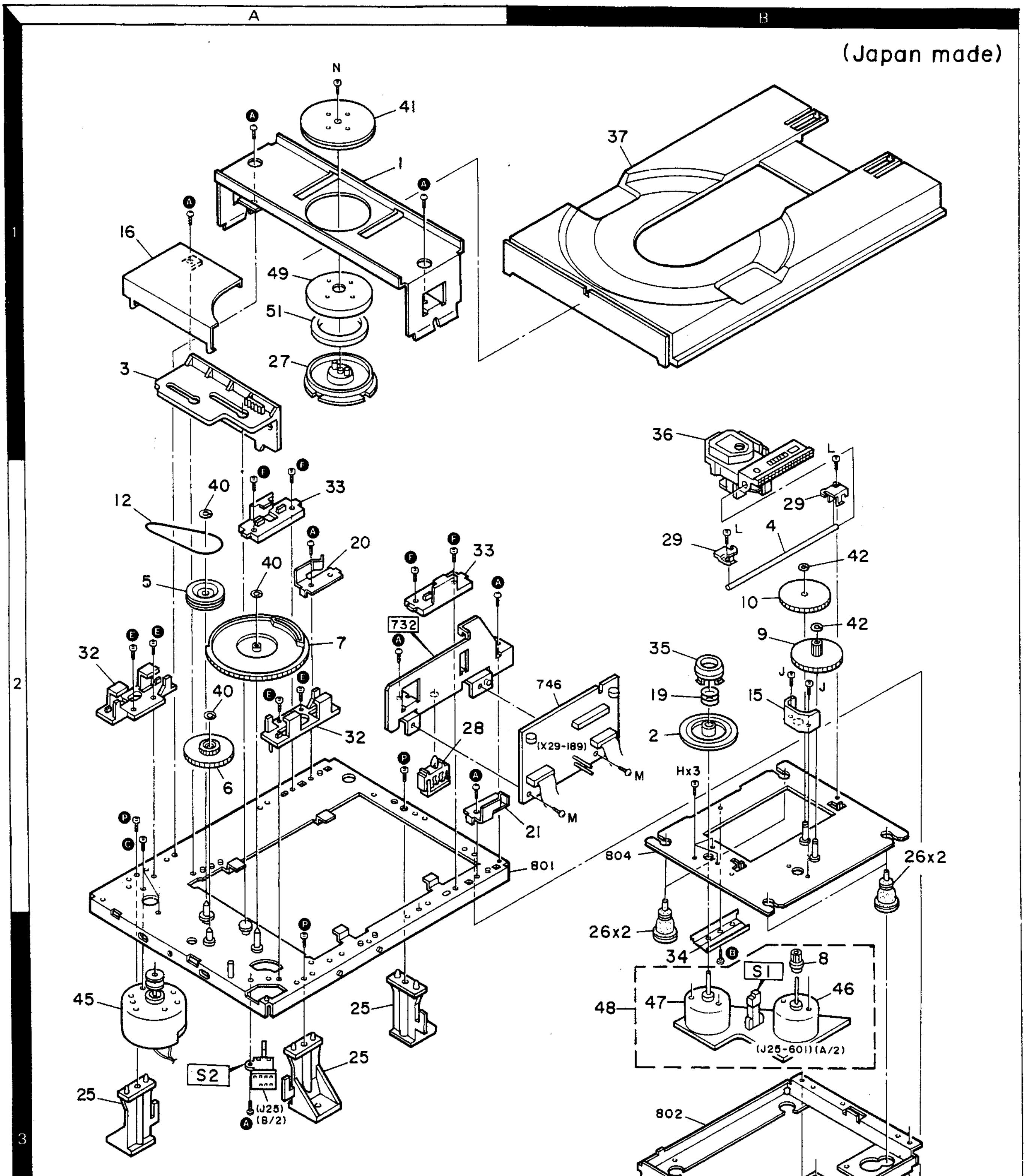
- Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen. Voltmeter gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen instrumenten oder Geräten u.U. geringfügig.

DP-720

KENWOOD

Y22-1532-71

EXPLODED VIEW (MECHANISM)

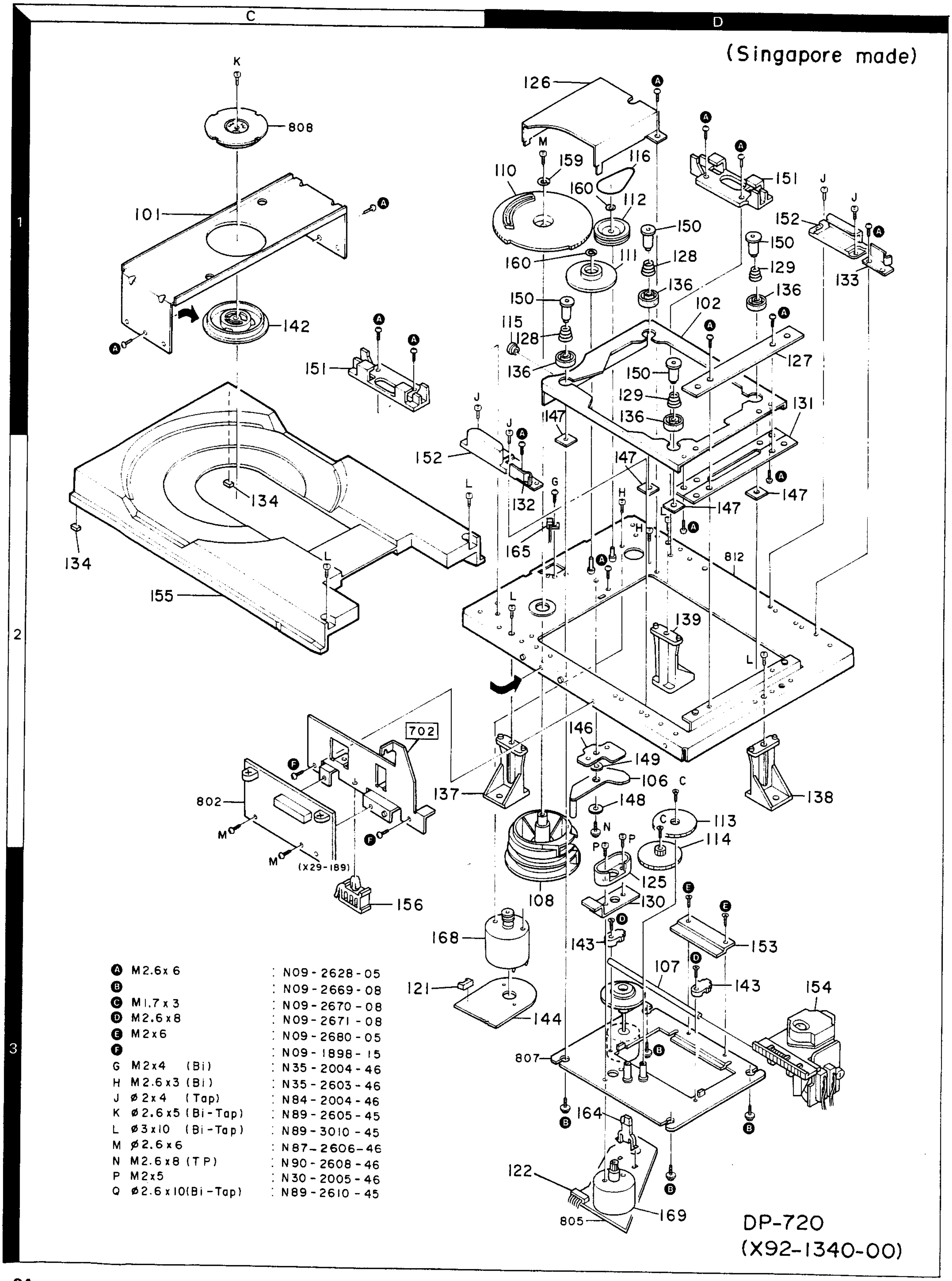


A			: N09 - 1898 - 15				
B			: N09 - 2613 - 05				
C			: N09 - 2627 - 05				
D			: N09 - 2628 - 05				
E	ø 2.6x6	(Bi - Tap)	: N86 - 2606 - 46	L	ø 2x6	(Tap)	: N84 - 2006 - 46
F	ø 2x4	(Tap)	: N84 - 2004 - 46	M	ø 2.6x6	(Br - Tap)	: N87 - 2606 - 46
H	M 2x2.5		: N39 - 2025 - 46	N	ø 2.6x6	(Bi - Tap)	: N89 - 2606 - 46
J	M 2x3.5	BLK	: N39 - 2035 - 45	P	ø 3x10	(Bi - Tap)	: N89 - 3010 - 46

DP-720
(X92-1300-00)

Parts with the exploded numbers larger than 700 are not supplied.

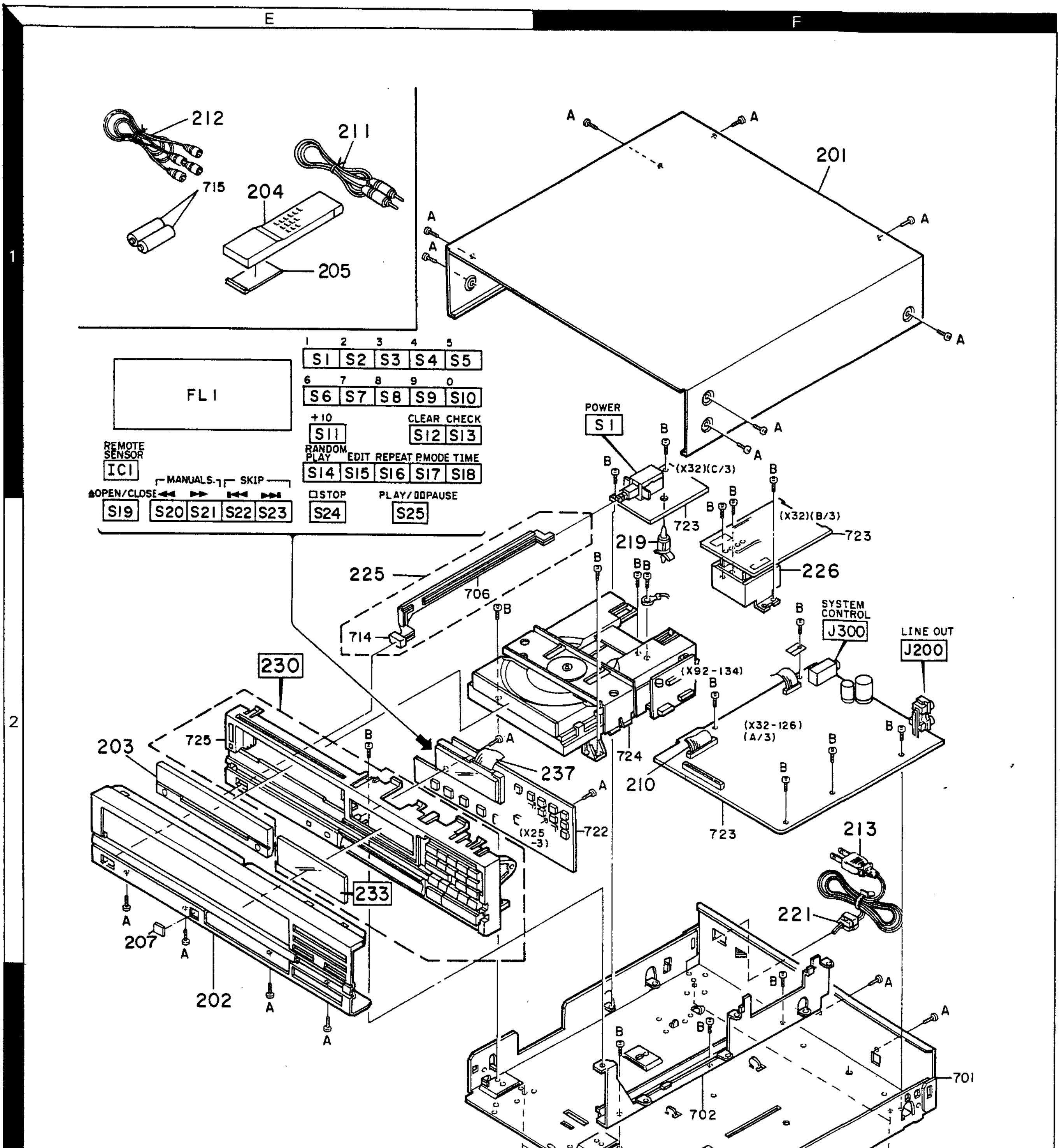
EXPLODED VIEW (MECHANISM)



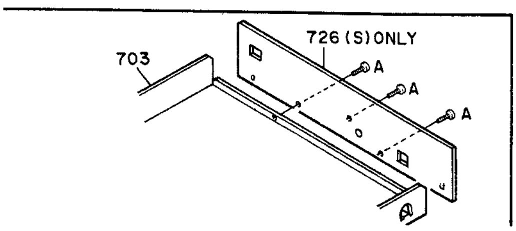
A	M2.6x6	: N09-2628-05
B		: N09-2669-08
C	M1.7x3	: N09-2670-08
D	M2.6x8	: N09-2671-08
E	M2x6	: N09-2680-05
F		: N09-1898-15
G	M2x4 (Bi)	: N35-2004-46
H	M2.6x3 (Bi)	: N35-2603-46
J	ø2x4 (Tap)	: N84-2004-46
K	ø2.6x5 (Bi-Tap)	: N89-2605-45
L	ø3x10 (Bi-Tap)	: N89-3010-45
M	ø2.6x6	: N87-2606-46
N	M2.6x8 (TP)	: N90-2608-46
P	M2x5	: N30-2005-46
Q	ø2.6x10(Bi-Tap)	: N89-2610-45

Parts with the exploded numbers larger than 700 are not supplied.

EXPLODED VIEW (UNIT)



A ø3x8 (Bi-Tap) BLK : N89-3008-45
B ø3x6 (Bi-Tap) : N89-3006-46
G ø3x8 : N09-1515-05



Parts with the exploded numbers larger than 700 are not supplied.

PARTS LIST

⁎ New Parts
Parts without Parts No. are not supplied.
Les articles non mentionnes dans le Parts No. ne sont pas fournis.
Teile ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
DP-720 (J : Japan made, S : Singapore made)						
201	1F	*	A01-1690-01	METALLIC CABINET		J
201	1F	*	A01-1705-01	METALLIC CABINET		S
202	2E	*	A20-5645-02	PANEL		
203	2E	*	A29-0133-03	PANEL (TRAY)		
204	1E	*	A70-0244-05	REMOTE CONTROLLER ASSY		
205	1E		A09-0076-08	BATTERY COVER(REMOTE CONTROL)		
230	2E		A22-1026-03	SUB PANEL ASSY		S
207	1E	*	B03-2498-04	DRESSING PLATE		
-			B46-0096-13	WARRANTY CARD	X	J
-			B46-0122-13	WARRANTY CARD	E	
-			B46-0143-03	WARRANTY CARD	T	
-		*	B50-9181-00	INSTRUCTION MANUAL		S
-		*	B50-9182-00	INSTRUCTION MANUAL	E	S
-		*	B50-9183-00	INSTRUCTION MANUAL	E	S
-		*	B50-9188-00	INSTRUCTION MANUAL		J
-		*	B50-9189-00	INSTRUCTION MANUAL	ME	J
-		*	B50-9190-00	INSTRUCTION MANUAL	E	J
-		*	B50-9191-00	INSTRUCTION MANUAL	M	J
210	2E		E31-4362-05	WIRING HARNESS		
211	2F		E30-1392-05	CORD WITH PLUG		
212	1E		E30-0615-05	AUDIO CORD		
⚠ 213	2F		E30-0459-05	AC POWER CORD	E	
⚠ 213	2F		E30-1341-05	AC POWER CORD	X	J
⚠ 213	2F		E30-1416-05	AC POWER CORD	T	
⚠ 213	2F		E30-2284-05	AC POWER CORD	M	J
-		*	H01-8318-04	ITEM CARTON CASE		J
-		*	H01-8319-04	ITEM CARTON CASE		S
-		*	H10-3688-12	POLYSTYRENE FOAMED FIXTURE		J
-		*	H10-3689-12	POLYSTYRENE FOAMED FIXTURE		J
-			H10-3690-02	POLYSTYRENE FOAMED FIXTURE		S
-			H10-3691-02	POLYSTYRENE FOAMED FIXTURE		S
-		*	H20-0554-14	PROTECTION COVER(460X370X360)	M	J
-			H25-0232-04	PROTECTION BAG (235X350X0.03)		
-			H25-0330-04	PROTECTION BAG (750X350X0.03)	XTE	J
-			H25-0330-04	PROTECTION BAG (750X350X0.03)		S
217	3E		J02-1003-05	FOOT (FRONT)		
218	3F		J02-0170-04	FOOT (REAR)		
219	2F		J19-0515-05	UNIT HOLDER		
⚠ 221	2F		J42-0083-05	POWER CORD BUSHING		S
⚠ 221	2F		J42-0166-05	POWER CORD BUSHING		J
225	2E		K29-3337-03	KNOB ASSY (POWER)		
⚠ 226			L01-5162-15	POWER TRANSFORMER		S
⚠ 226	2F		L01-5162-15	POWER TRANSFORMER	XTE	J
⚠ 226	2F		L01-5164-15	POWER TRANSFORMER	M	J
G	3E,3F		N09-1515-05	TAPPING SCREW (Ø3X8)		
OPERATION UNIT (X25-34XX-XX) 60-01 : J, 72-71 : S						
230	2E		A22-1015-03	SUB PANEL ASSY		J
233	2F		B03-2490-04	DRESSING PLATE		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE : AAFES(Europe) X: Australia

J : Japan made (M, X, T, E type)
S : Singapore made (T, E type)

⚠ indicates safety critical components.

PARTS LIST

⁎ New Parts
Parts without Parts No. are not supplied.
Les articles non mentionnes dans le Parts No. ne sont pas fournis.
Teile ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
237	2F		E31-4697-05	WIRING HARNESS		
CN1			E10-2904-05	FLAT CABLE CONNECTOR		
S1 -25			S40-1064-05	PUSH SWITCH		
A1			GP-1U501	IC(REMOTE SENSOR)		S
D1 -7			HSS104A	DIODE		
D1 -7			1SS131	DIODE		
FL1			FIP10AM19	FLUORESCENT INDICATOR TUBE		
IC1			GP-1U501	IC(REMOTE SENSOR)		J
CONTROL CIRCUIT UNIT (X29-1890-XX) -02 : J, -03 : S						
C1			CE04JW1A101M	ELECTRO 100UF 10WV		
C2			CF92FV1H682J	MF 6800PF J		
C3			CC45FSL1H120J	CERAMIC 12PF J		
C4			CC45FSL1H150J	CERAMIC 15PF J		
C5			CC45FSL1H150J	CERAMIC 15PF J		
C6			CE04JW1E330M	ELECTRO 33UF 25WV		
C7			CF92FV1H333J	MF 0.033UF J		
C8			CF92FV1H103J	MF 0.010UF J		
C9			CF92FV1H333J	MF 0.033UF J		
C10 ,11			CE04KW1C470M	ELECTRO 47UF 16WV		
CN3			E10-1705-05	FLAT CABLE CONNECTOR		
L1			L40-1001-17	SMALL FIXED INDUCTOR(10UH,K)		
VR1			R12-3100-05	TRIMMING POT.(10K) FE BALANCE		
VR2			R12-3101-05	TRIMMING POT.(22K) TE BALANCE		
D1			1SS133	DIODE		
D1			1SS176	DIODE		
IC1			CXA1081M	IC(RF AMP)		
Q1			2SA1426	TRANSISTOR		
Q2			2SC945(A)(Q,P)	TRANSISTOR		
CD PLAYER UNIT (X32-XXXX-XX) -1260-23 : J(M), -1262-73 : J(X,T,E), -1302-72 : S(T,E)						
C1			CF92FV1H333J	MF 0.033UF J		
C2			CF92FV1H472J	MF 4700PF J		
C3			CK45FF1H223Z	CERAMIC 0.022UF Z		
C4			C91-0085-05	CERAMIC 0.022UF N		
C5			CF92FV1H104J	MF 0.10UF J		
C6			CF92FV1H102J	MF 1000PF J		S
C6			CF92FV1H222J	MF 2200PF J		J
C7			C90-1349-05	NP-ELEC 1UF 50WV		
C8			CF92FV1H184J	MF 0.18UF J		S
C8			CF92FV1H274J	MF 0.27UF J		J
C9			CF92FV1H273J	MF 0.027UF J		
C10			CF92FV1H243J	MF 0.024UF J		
C11			C90-1335-05	NP-ELEC 4.7UF 50WV		S
C11			C90-1352-05	NP-ELEC 4.7UF 25WV		J
C12			CC45FSL1H101J	CERAMIC 100PF J		
C13			CF92FV1H224J	MF 0.22UF J		
C14			CF92FV1H473J	MF 0.047UF J		
C15			CC45FSL1H181J	CERAMIC 180PF J		
C16			CE04KW1V4R7M	ELECTRO 4.7UF 35WV		
C17			CF92FV1H122J	MF 1200PF J		
C18			CE04KW1V4R7M	ELECTRO 4.7UF 35WV		
C19 ,20			CF92FV1H103J	MF 0.010UF J		
C21			C90-1332-05	NP-ELEC 10UF 25WV		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE : AAFES(Europe) X: Australia

J : Japan made (M, X, T, E type)
S : Singapore made (T, E type)

⚠ indicates safety critical components.

PARTS LIST

⁎ New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
C22			C91-0763-05	CERAMIC 0.0033UF M		
C23			C90-1332-05	NP-ELEC 10UF 25WV		
C24			C91-0757-05	CERAMIC 1000PF K		
C25			CC45FSL1H331J	CERAMIC 330PF J		
C26			CC45FSL1H101J	CERAMIC 100PF J		
C27			C90-1350-05	NP-ELEC 2.2UF 50WV		
C30			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C31			CK45FB1H102K	CERAMIC 1000PF K		
C32			CE04KW0J221M	ELECTRO 220UF 6.3WV		
C33 ,34			CF92FV1H103J	MF 0.010UF J		
C35			CF92FV1H332J	MF 3300PF J		
C36		*	C91-0759-05	CERAMIC 0.0015UF M		
C37			C91-0085-05	CERAMIC 0.022UF N		
C38			CF92FV1H563J	MF 0.056UF J		
C39			CC45FSL1H101J	CERAMIC 100PF J		
C40 ,41			CF92FV1H222J	MF 2200PF J		
C42			CC45FUJ1H050C	CERAMIC 5.0PF C		
C43			CC45FUJ1H221J	CERAMIC 220PF J		
C44			CC45FUJ1H330J	CERAMIC 33PF J		
C45			CF92FV1H103J	MF 0.010UF J		
C46			CE04KW1HR47M	ELECTRO 0.47UF 50WV		
C48			CE04KW1A470M	ELECTRO 47UF 10WV		
C49			CF92FV1H473J	MF 0.047UF J		
C50			C91-0769-05	CERAMIC 0.01UF M		
C51 ,52			CK45FF1H223Z	CERAMIC 0.022UF Z		
C53 ,54			CK45FB1H102K	CERAMIC 1000PF K		
C55			CK45FF1H223Z	CERAMIC 0.022UF Z		
C56			CK45FB1H102K	CERAMIC 1000PF K		
C59			C91-0757-05	CERAMIC 1000PF K		
C60 ,61			CC45FSL1H070D	CERAMIC 7.0PF D		
C62			CF92FV1H472J	MF 4700PF J		
C63 -66			CQ09FS1H182JZS	POLYSTY 1800PF J		
C67 ,68			CE04KW1V4R7M	ELECTRO 4.7UF 35WV		
C69 ,70			CF92FV1H562J	MF 5600PF J		
C71 ,72			CF92FV1H273J	MF 0.027UF J		
C73 ,74			CC45FSL1H331J	CERAMIC 330PF J		
C75 ,76			CF92FV1H562J	MF 5600PF J		
C77 ,78			CF92FV1H273J	MF 0.027UF J		
C79 ,80			CC45FSL1H271J	CERAMIC 270PF J		
C81 ,82			CF92FV1H273J	MF 0.027UF J		
C83 ,84			CE04KW1V4R7M	ELECTRO 4.7UF 35WV		
C85 ,86			CF92FV1H222J	MF 2200PF J		
C87			CE04KW1V100M	ELECTRO 10UF 35WV		
C88			CE04KW1C331M	ELECTRO 330UF 16WV		
C100			CE04KW1C332M	ELECTRO 3300UF 16WV		
C101			CE04KW1C222M	ELECTRO 2200UF 16WV		
C102-105			CE04KW1A470M	ELECTRO 47UF 10WV		
C106			CE04KW0J331M	ELECTRO 330UF 6.3WV		
C107			CE04KW1A470M	ELECTRO 47UF 10WV		
C108,109			CE04KW1C330M	ELECTRO 33UF 16WV		
C110			CE04KW1H470M	ELECTRO 47UF 50WV		
C111,112			CK45FF1H223Z	CERAMIC 0.022UF Z		
C113			CE04KW1C221M	ELECTRO 220UF 16WV		
C114			CK45FF1H223Z	CERAMIC 0.022UF Z		
C115			C91-0085-05	CERAMIC 0.022UF N		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

J : Japan made (M, X, T, E type)
S : Singapore made (T, E type)

⚠ indicates safety critical components.

DP-720

PARTS LIST

⁎ New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

	Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
⚠	C116			C91-0647-05	CERAMIC 0.01UF P		
⚠	C117,118			C91-0647-05	CERAMIC 0.01UF P	M	J
⚠	C117,118			C91-0647-05	CERAMIC 0.01UF P		S
⚠	C119,120			C91-0647-05	CERAMIC 0.01UF P	XTE	J
	CN1			E10-1705-05	FLAT CABLE CONNECTOR		
	CN5			E10-2903-05	FLAT CABLE CONNECTOR		
	J200			E13-0235-05	PHONO JACK (2P) LINE OUT		
	J300			E11-0164-05	MINIATURE PHONE JACK(SYSTEM CN		
	L1		*	L32-0355-05	OSCILATING COIL (VCO)		
	L2			L40-1092-17	SMALL FIXED INDUCTOR(1UH,M)		
⚠	L3			L79-0733-05	LINE FILTER	M	J
⚠	L3			L79-0733-05	LINE FILTER		S
⚠	L4			L79-0733-05	LINE FILTER	XTE	J
	X2			L77-1128-05	CRYSTAL RESONATOR		
	R55 ,56			RS14KB3A150J	FL-PROOF RS 15 J 1W		
	R60			RS14KB3A180J	FL-PROOF RS 18 J 1W		J
	R80 ,81			RS14KB3A8R2J	FL-PROOF RS 8.2 J 1W		
	VR1 ,2			R12-3126-05	TRIMMING POT.(10K) F/T GAIN		
⚠	S1	1F		S40-1103-05	PUSH SWITCH (POWER)		
⚠	S2			S31-2131-05	SLIDE SWITCH (POWER TYPE)	M	J
	D1 -3			HSS104	DIODE		
	D1 -3			1SS133	DIODE		
	D4			1SV147	VARISTOR		
	D5 -11			HSS104	DIODE		
	D5 -11			1SS133	DIODE		
	D12			HSS104A	DIODE		
	D12			1SS131	DIODE		
	D13			HSS104A	DIODE		S
	D13			1SS131	DIODE		S
	D14			HSS104	DIODE		
	D14			1SS133	DIODE		
	D15			HZS8.2S(B2)	ZENER DIODE		
	D15			RD8.2JS(B2)	ZENER DIODE		
	D16 -19			S5566B	DIODE		
	D20 ,21			HSS104	DIODE		
	D20 ,21			1SS133	DIODE		
	D22			S5566B	DIODE		
	D23 ,24			HSS104	DIODE		
	D23 ,24			1SS133	DIODE		
	D25		*	HZS30S(B)	ZENER DIODE		
	D25		*	RD30JS(B)	ZENER DIODE		
	D26			HZS5.6S(B2)	ZENER DIODE		
	D26			RD5.6JS(B2)	ZENER DIODE		
	D27			HZS3.3N(B2)	ZENER DIODE		
	D27			RD3.3ES(B2)	ZENER DIODE		
	D28			HSS104	DIODE		
	D28			1SS133	DIODE		
	D29			HZS4.7N(B)	ZENER DIODE		
	D29			RD4.7ES(B)	ZENER DIODE		
	D30			HSS104	DIODE		
	D30			1SS133	DIODE		
	D31			HSS104A	DIODE		S
	D31			1SS131	DIODE		S

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

J : Japan made (M, X, T, E type)
S : Singapore made (T, E type)

⚠ indicates safety critical components.

PARTS LIST

⁎ New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Desti-nation 仕向	Re-marks 備考
D32 ,33			HSS104	DIODE		
D32 ,33			1SS133	DIODE		
D34 ,35			S5566B	DIODE		
IC1			TC4066BP	IC(ANALOG/ DIGITAL SW)		
IC2			CXA1244S	IC(SERVO SIGNAL PROCESSOR)		
IC3			M5218P	IC(OP AMP X2)		
IC4		*	CXD1135Q	IC(DIGITAL SIGNAL PROCESSOR)		
IC4			CXD1135QZ	IC(DIGITAL SIGNAL PROCESSOR)		
IC5			LC3518BSL-15	IC(2KX8 RAM)		
IC6			M5218P	IC(OP AMP X2)		
IC7		*	UPD75212ACW-028	IC(MICROPROCESSOR)		
IC8			TD6720N	IC(16BIT HI-FI D/A CONVERTER)		
IC9 ,10			M5218P	IC(OP AMP X2)		
IC11			LM2940CT-5.0	IC(LOW VOLTAGE REGULATOR)		
IC12			M5218P	IC(OP AMP X2)		
Q1			2SA733(A)(Q,P)	TRANSISTOR		
Q1			2SA933S(Q,R)	TRANSISTOR		
Q2			2SC1740S(Q,R)	TRANSISTOR		
Q2			2SC945(A)(Q,P)	TRANSISTOR		
Q3			2SD1266	TRANSISTOR		
Q4			2SA1534A	TRANSISTOR		
Q5			STA341M	TRANSISTOR		
Q6			2SC1740S(Q,R)	TRANSISTOR		
Q6			2SC945(A)(Q,P)	TRANSISTOR		
Q7			2SC3940A	TRANSISTOR		
Q8			2SA1534A	TRANSISTOR		
Q9 -12			2SC2878(B)	TRANSISTOR		
Q13			2SA733(A)(Q,P)	TRANSISTOR		
Q13			2SA933S(Q,R)	TRANSISTOR		
Q14			2SC1740S(Q,R)	TRANSISTOR		
Q14			2SC945(A)(Q,P)	TRANSISTOR		
Q15			2SD1944	TRANSISTOR		
Q16 -18			2SA954(L,K)	TRANSISTOR		
Q19 ,20			2SC2878(B)	TRANSISTOR		
MECHANISM ASS'Y (X92-1300-00) : Japan made						
1	1A		A11-0278-03	SUB CHASSIS		
2	2B	*	D02-0086-08	TURNTABLE PLATTER		
3	1A		D10-2227-03	SLIDER		
4	2B	*	D10-2249-04	ROD		
5	2A		D13-0722-04	GEAR		
6	2A		D13-0723-04	GEAR		
7	2A		D13-0724-03	GEAR		
8	3B	*	D13-0745-08	GEAR		
9	2B	*	D13-0746-08	GEAR		
10	2B	*	D13-0747-04	GEAR		
12	2A		D16-0191-04	BELT		
15	2B	*	F07-0546-08	COVER		
16	1A		F19-0571-04	BLIND PLATE		
17	3B	*	F31-0182-04	REINFORCING HARDWARE		
19	2B	*	G01-2308-08	COMPRESSION SPRING		
20	2A		G02-0493-04	FLAT SPRING (L)		
21	2A		G02-0494-04	FLAT SPRING (R)		
22	3B		G02-0495-08	FLAT SPRING		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE : AAFES(Europe) X: Australia

J : Japan made (M, X, T, E type)
S : Singapore made (T, E type)

⚠ indicates safety critical components.

PARTS LIST

⁎ New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Desti-nation 仕向	Re-marks 備考
25	3A		J02-0386-04	FOOT		
26	2B,3B		J02-0387-05	INSULATOR		
27	1A		J11-0130-03	CLAMPER		
28	2A		J11-0134-05	WIRE CLAMPER		
29	2B	*	J19-3083-03	HOLDER		
32	2A		J90-0617-03	GUIDE		
33	2A		J90-0618-03	GUIDE		
34	3B	*	J90-0623-08	RAIL		
35	2B	*	J90-0624-08	GUIDE		
36	1B	*	J91-0372-05	PICKUP		
37	1B		J99-0053-01	TRAY		
40	2A		N19-0891-04	FLAT WASHER		
41	1A		N19-1170-04	FLAT WASHER		
42	2B	*	N19-1179-05	FLAT WASHER		
A			N09-1898-15	MACHINE SCREW		
B		*	N09-2613-05	SEMS (TAPTITE SCREW)		
C		*	N09-2627-05	MACHINE SCREW		
D		*	N09-2628-05	MACHINE SCREW		
S1	3B	*	S46-1122-05	LEAF SWITCH		
S2	3A		S33-2060-05	LEVER ROTARY SWITCH		
45	3A		T42-0483-05	DC MOTOR		
46	3B	*	T42-0495-05	DC MOTOR		
47	3B	*	T42-0496-05	DC MOTOR		
48	3B	*	T42-0497-08	MOTOR ASSY		
49	1A		T50-1036-04	YOKE		
51	1A		T99-0222-05	MAGNET		
MECHANISM ASS'Y (X92-1340-00) : Singapore made						
101	1C		A11-0617-08	SUB CHASSIS ASSY		
102	2D		A11-0618-08	SUB CHASSIS ASSY		
106	2D	*	D10-2314-08	STOPPER LINK ASSY		
107	3D		D10-2315-08	ROD		
108	3D	*	D12-0126-08	CONTROL CAM		
110	1C	*	D13-0799-08	DRIVE GEAR		
111	1D	*	D13-0800-08	GEAR		
112	1D	*	D13-0801-08	DOADING PULLEY		
113	2D		D13-0802-08	GEAR (A)		
114	2D		D13-0803-08	GEAR (B)		
115	1D	*	D14-0300-08	ROLLER		
116	1D	*	D16-0276-08	BELT (M)		
121	3C		E40-3263-05	CONNECTOR (5P)		
122	3C,3D	*	E40-3262-05	CONNECTOR (4P)		
125	3D		F07-0554-08	COVER (GEAR)		
126	1D	*	F19-0595-08	COVER (GEAR)		
127	1D	*	F31-0187-08-	REINFORCING HARDWARE		
130	3D	*	F31-0188-08	STOPPER		
128	1D	*	G01-2375-08	COMPRESSION SPRING (A)		
129	1D	*	G01-2376-08	COMPRESSION SPRING (B)		
131	1D	*	G02-0917-08	SPRING		
132	2D	*	G02-0918-08	TRAY GUIDE SPRING (R)		
133	1D	*	G02-0919-08	TRAY GUIDE SPRING (L)		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE : AAFES(Europe) X: Australia

J : Japan made (M, X, T, E type)
S : Singapore made (T, E type)

⚠ indicates safety critical components.

PARTS LIST

⁎ New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Desti-nation 仕向	Re-marks 備考
134	2C	*	G13-0237-08	CUSHION		
136	1D	*	J02-1019-08	INSULATOR		
137	2C	*	J02-1020-08	FOOT (R)		
138	2D	*	J02-1021-08	FOOT (REAR)		
139	2D	*	J02-1022-08	FOOT (L)		
142	1C	*	J11-0145-08	CLAMPER		
143	3D		J19-3148-08	HOLDER (ROD)		
144	3D	*	J25-6134-08	PRINTED WIRING BOARD(MOTOR)		
146	2D	*	J30-0261-08	SPACER		
147	2D	*	J30-0262-08	SPACER		
148	2D	*	J30-0263-08	SPACER		
149	2D	*	J32-0828-08	BOSS		
150	1D	*	J42-0619-08	BUSHING		
151	1C,1D	*	J90-0638-08	GUIDE (FRONT)		
152	2C,1D	*	J90-0639-08	GUIDE (REAR)		
153	3D		J90-0640-08	GUIDE (SLIDE)		
154	3D	*	J91-0385-08	PICK UP		
155	2C	*	J99-0064-08	TRAY		
156	3C		J11-0134-05	WIRE CLAMPER		
			J61-0307-05	WIRE BAND		
159	1D	*	N19-1208-08	FLAT WASHER		
160	1D	*	N19-1209-08	FLAT WASHER		
A	1C,1D		N09-2628-05	SCREW		
B	3D	*	N09-2669-08	SCREW		
C	2D		N09-2670-08	SCREW (M1.7X3)		
D	3D		N09-2671-08	SCREW		
E	3D		N09-2680-05	SCREW		
F	2C		N09-1898-15	MACHINE SCREW		
164	3D		S46-1128-08	LEAF SWITCH		
165	2D	*	S46-2109-08	LEAF SWITCH		
168	3D	*	T42-0526-08	MOTOR ASSY (LOADING)		
169	3D	*	T42-0527-08	MOTOR ASSY (SLED)		

E: Scandinavia & Europe　K: USA　P: Canada
U: PX(Far East, Hawaii)　T: England　M: Other Areas
UE: AAFES(Europe)　X: Australia

J : Japan made (M, X, T, E type)
S : Singapore made (T, E type)

⚠ indicates safety critical components.

SPECIFICATIONS

[Format]

Type: .... Compact disc player
Read system: .... Non-contact optical pickup
Rotational speed: .... About 200 to 500 rpm

[Audio]

Frequency response: .... 20Hz ~ 20kHz
Signal-to-noise ratio: .... more than 91dB
Total harmonic distortion: .... 0.01% at 1kHz
Channel separation: .... more than 90dB at 1kHz
Wow flutter: .... Below measurable limit
Output level/impedance: .... 1.2V/2.2 kohms

[General]

Power consumption: 12W
Dimensions: .... W: 360mm
H: 95mm
D: 352mm
Weight: 4.2kg

Note:
KENWOOD follows a policy of continuous development. For this reason specifications may be changed without notice.

Note :
Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on, the Europe (E) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

KENWOOD CORPORATION